



CADENCE AND NEWPORT MEDIA

Newport Media Pinpoints Design Bugs Earlier with Cadence Assertion Based VIP and Incisive Formal Verifier.

“Using Assertion Based VIP and IFV, we start verification earlier and find bugs much more efficiently. Obviously when we improve our productivity we accelerate our schedule.”

Sang Tran, Manager VLSI Technology, Newport Media

CORPORATE PROFILE

- Newport Media is a fabless semiconductor company that supplies highly integrated receiver solutions for emerging digital audio and mobile TV broadcast applications

DESIGN CHALLENGE

- Expose hard-to-find bugs early in the design cycle of AHB master/slave to verify protocol compliance
- Write more extensive tests to uncover and explore corner cases

CADENCE SOLUTION

- The Cadence Incisive Formal Verifier solution including Assertion Based Verification IP (VIP) were used to improve the productivity and quality of functional verification earlier in the design and verification process

CADENCE PRODUCTS

- Cadence Incisive Formal Verifier (IFV) and Cadence Incisive Assertion Based Verification IP (VIP)

DEVELOPING MOBILE TV TECHNOLOGY

Southern California’s Newport Media was founded in 2005 with the goal of delivering highly integrated receiver solutions for emerging digital audio and mobile TV applications. A fabless semiconductor company, Newport Media’s development team focuses on developing broadcast multimedia architectures and IC implementations with unprecedented performance, power consumption, size and cost-efficiency.

The company’s premier product line, Sundance Series, is a multi-standard platform developed to support a wide variety of emerging mobile television standards, including DVB-H, DMB, ISDB-T and FLO. The single-chip RF tuner delivers an advanced user feature set and best-in-class RF noise figure and demodulator Doppler performance.

Newport Media’s Sang Tran was tasked with developing the verification environment for a new version of the design

featuring an external bus interface. The block verified featured 40K logic gates, including an AHB master/slave interface, an external microprocessor interface, and a DMA engine. “We wanted to address some difficult challenges,” said Tran. “In addition to speeding up the verification process, we aimed to write more extensive tests to uncover and explore corner cases.”

INSTANT AND INSIGHTFUL FEEDBACK

Though Tran and his team had prior experience with another formal verification tool, they opted to employ the Cadence® Incisive® Formal Verifier (IFV) solution and Cadence Incisive Assertion Based Verification IP (VIP). “I believe each solution has merit, but the Cadence solution really does provide a validated verification approach,” said Tran. “I like how the VIP provides instantaneous feedback indicating whether the design complies with the AHB master/slave protocol being tested.”

"I brought up the verification environment in just 15 minutes. I can say confidently that Cadence's AHB verification IP saved me several weeks, at a minimum."

Sang Tran, Manager VLSI Technology, Newport Media

Tran said he had previous experience with verification IP, but found it hard to understand. "In the past I had to treat it as a black box," he said. "This time I found it be a much more pleasant experience because I could follow the assertions inside the VIP as if they were in plain English. This solution gives me very clear insight into what each assertion covers."

MAKING QUICK WORK OF VERIFICATION

The Newport Media verification team took advantage of Cadence's AHB Assertion Based VIP offering, part of Cadence's extensive Plan-to-Closure VIP portfolio. The AHB VIP, a plug-and-play verification environment that was developed together with ARM, simplifies verification for the AMBA AHB protocol. "It is quite amazing," said Tran. "I brought up the verification environment in just 15 minutes." The VIP provides static analysis and protocol compliance checking. Tran was fast to profess the VIP provided a serious short cut. "It's a bit difficult to say exactly how much time it might have taken to create the verification environment myself because that

would depend on what kind of test coverage I was aiming to achieve. However, I can say confidently that the Cadence verification component saved me several weeks, at a minimum."

INCREASED PREDICTABILITY, DECREASED RISK

Newport Media employed the Cadence Incisive Formal Verifier (IFV) solution, together with the Assertion Based VIP to enable engineers to begin module verification at the very same time they're being designed. This reduces re-spins and lowers risk. Tran did indeed realize these benefits. "I would definitely say we increased our quality and predictability. We saved weeks of engineering time."

Tran said it typically might take weeks to detect hard-to-find corner cases. He stated that IFV accurately pinpointed design bugs in about an hour. Because formal analysis does not require the use of test vectors, functional bugs can be detected months before testbench development and simulation can begin.

IFV AND VIP NOW A FIXTURE AT NEWPORT MEDIA

Tran said his first experience with Cadence IFV and VIP was a valuable one. "We learned a lot. We can start verification earlier in the process and find bugs much more efficiently. Obviously when we improve our productivity we accelerate our schedule." Will the Newport Media team be using a similar set of tools for the next verification task? "Yes indeed," said Tran. "We're happy with how IFV increased our verification productivity. As long as the relevant VIP is available for our next project we'll employ much of the same processes."

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