

Kilopass Technology and Cadence

“We needed a design flow that automated some of the manual layout task of building our newest 4Mb Gusto memory, the industry’s highest capacity one-time programmable, non-volatile memory IP block. Using Cadence Virtuoso 6.1 technology, we shortened our 9-month design-to-tapeout cycle by several weeks.”
 Bill Ip, Principal Engineer, Kilopass Technology, Inc.

The Customer

Kilopass Technology, Inc. develops leading-edge one-time programmable (OTP) non-volatile memory (NVM) intellectual property (IP) blocks for system-on-chip (SoC) applications. The company produces and sells hard IP in the form of GDSII files to fabless and integrated device manufacturer (IDM) customers. Kilopass memory is used to safeguard firmware and to store security codes, calibration data, and other application-critical information. More than a dozen foundries and IDMs have relied on Kilopass IP in more than 800,000 shipped wafers.

The Challenge

Kilopass develops their OTP NVM blocks in standard logic CMOS processes from 180nm to 28nm, and their extra-permanent XPM memory family ranges up to 1Mb. But for their latest offering, the Gusto product line, Kilopass engineers were tasked with developing the industry’s first 4Mb embedded OTP NVM.

Such complex design requirements posed a challenge to achieving tapeout in a 9-month window. The time needed to manually create the 4 million bit cells and associated logic in the largest version of Gusto memory would be prohibitive. And about 10 percent of the design would require the layout team to import GDSII developed by third-party contractors. Kilopass needed a solution that automated layout, optimized communications among designers and implementation engineers, and enabled them to support multiple foundries and process nodes.

Business Challenges

- Meet an aggressive 9-month tapeout schedule on a new product line
- Implement memory blocks at the most demanding process nodes from multiple foundries

Design Challenges

- Boost layout productivity
- Improve communication between designers and implementation engineers
- Quickly migrate from one process node for a given foundry to the next generation using a standard CMOS process

Cadence Solutions

- Virtuoso unified custom/analog flow (6.1)
- OpenAccess database

Results

- Increased layout productivity through automation
- Maintained consistency and preserved design intent on critical pieces of the design
- Support for multiple foundries, different design flows, and various process nodes
- Shortened the tapeout schedule by several weeks

The Solution

"Kilopass was a Cadence OpenChoice customer in 2003 and Cadence technologies were instrumental in helping Kilopass get started and grow," explains Bill Ip, Principal Engineer at Kilopass. Familiar with the benefits of Cadence technology, Kilopass selected the Virtuoso® 6.1 unified custom/analog flow to help them build the 4Mb Gusto product line.

The Virtuoso flow reduced the layout burden facing the Kilopass implementation team by automating what were once repetitive and error-prone manual tasks. Bill Ip cites Virtuoso Design Navigator, Property Editor, Search Assistant, and World View Assistant functionalities as especially helpful in boosting layout productivity.

"Thanks to Virtuoso 6.1, the task of conversion takes half the time compared to starting from scratch."

For example, labeling the bit line, word line, sense amplifier, and power and ground for a 4Mb memory would take considerable time if done manually. With Virtuoso 6.1, the task is simple. In a pull-down menu, the implementation engineer completes a form that asks for the signal name, the number of pins to be labeled, the x and y coordinates of the first signal, the spacing between the pins, and the size of the text. The Virtuoso tool then labels all the signal names.

The task of importing the existing layout into Virtuoso 6.1 was greatly eased by the technology's support of the OpenAccess database. Netlists from contractors working on a variety of different front-end tools could be easily imported into Virtuoso 6.1 for integration into the larger Gusto memory design.

Support for Multiple Foundries

Kilopass supports several foundries. Once the Gusto memory block was implemented in Foundry A's 45nm process, the Kilopass layout team needed to convert the memory to 45nm at Foundry B. This task is simple with Virtuoso 6.1 because of its support of the OpenAccess database, which is being adopted by most major foundries.

Using the Virtuoso flow, conversion is a two-step process: layer mapping followed by data manipulation. "Thanks to Virtuoso 6.1, the task of conversion takes half the time compared to starting from scratch," says Ip.

In the first step, a mapping table is entered into the Virtuoso environment that replaces Foundry A's 45nm library with Foundry B's 45nm library. The tool then produces a layout for Foundry B and highlights the exceptions it encounters in the process. In the second step, the implementation engineer examines these exceptions (for example, Foundry B required an additional layer to create the bit cell) and then makes the necessary adjustments (i.e., manipulates the data). Once the conversion is complete, a design-rule-check is performed along with final verification.

Results

Virtuoso 6.1 accelerated layout through higher levels of automation and handy docked assistants around the layout canvas, helping Kilopass shave several weeks off their 9-month tapeout schedule for an entire line of new memory IP. With a unified custom/analog flow and OpenAccess database integration, Kilopass had the flexibility to implement memory blocks ranging in capacity up to 4Mb for multiple foundries at various process nodes.



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