



CADENCE AND INPHI CORPORATION

Inphi Achieves Timing Closure and 1st Silicon Success® Using Encounter RTL Compiler Global Synthesis and SoC Encounter RTL-to-GDSII System

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Gopal Raghavan, *Founder and CTO, Inphi Corporation*

CORPORATE PROFILE

- Inphi Corporation delivers highspeed precision electronic components for computing, communications, and instrumentation systems

DESIGN CHALLENGE

- Achieve 666 MHz in a complex 130-nm mixed-signal design
- Adopt a solution to overcome challenges in floorplanning and routing

CADENCE SOLUTION

- Enabled accelerated turnaround time in the design using Cadence® Encounter® RTL Compiler global synthesis
- Automatic RDL routing using SoC Encounter flip-chip router helped team meet schedule

CADENCE PRODUCTS AND SERVICES

- Cadence Encounter digital IC design platform

PRECISION TIMING TO HELP YOU THINK FAST

Founded in 2000, California-based Inphi Corporation is a fabless electronic components company specializing in high-speed analog design and packaging. The company offers more than 80 off-the-shelf and customized components for the timing, instrumentation, optical, and microwave communication markets. Inphi’s custom devices can create a significant time-to-market advantage for their customers.

Inphi’s ExacTik family of CMOS timing devices is tailored to meet precision timing requirements for computing applications. The ExacTik design team was embarking on development of their latest offering, the ExacTik INAMB581 server memory chip. This new chip would include industry-first advanced memory buffer (AMB) extensions that would deliver higher performance with lower latency and power consumption. “We knew that we would be facing a

significant design challenge, but we see AMB as a key enabling technology for the future of the computing industry,” said Gopal Raghavan, Founder and CTO, Inphi Corporation.

ENCOUNTER PLATFORM ADDS DIGITAL PUNCH TO INPHI ANALOG FLOW

The Inphi design team needed to augment their analog flow to address the significant digital design hurdles they would be facing. “Our goal was to achieve a frequency target of 666 MHz on the digital side of the design, which was really pushing the envelope at 130nm,” continued Raghavan. “On top of that, we were dealing with some major hurdles in floorplanning and placement, with a 529-pin flip-chip package.” They had adopted the Cadence Encounter digital IC design platform a year earlier, primarily for synthesis, and decided to leverage more elements of the platform to meet their challenges.

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Gopal Raghavan, Founder and CTO, Inphi Corporation

CADENCE ENCOUNTER DIGITAL IC DESIGN PLATFORM POSITIONS INPHI FOR CONTINUED SUCCESS

"We had great success using the Cadence Encounter digital IC design platform," said Raghavan. "One of our biggest concerns was meeting timing on that part of the design. We optimized the design using Encounter RTL Compiler global synthesis, which enabled us to do lots of experimentation and helped with timing closure. In addition, the automatic RDL routing for flip chips in the SoC Encounter system kept us on schedule."

The Inphi team is now positioned to take on tough design challenges in both the analog and digital domains. "The silicon came back and the lab tests showed that the first spin was a success," said Raghavan. "Most importantly for us, the digital part of the chip met timing on the first pass. This was a major success for our team, to have accomplished so much in digital design when our expertise resides in analog." The team plans to continue to build on their skills using the Encounter digital IC design platform to meet the next big challenge.

ADDRESSING AGGRESSIVE FREQUENCY TARGET WITH ENCOUNTER RTL COMPILER GLOBAL SYNTHESIS

To address their 666-MHz goal, the Inphi team started by using Encounter RTL Compiler for synthesis and optimization. "We knew from the start that we were pushing the boundaries for a 130-nm process with this goal," said Raghavan. "But we were able to leverage the global synthesis capabilities in Encounter RTL Compiler to optimize our design quickly, giving us time to experiment and achieve high-quality results in timing, area, and power."

Another key element in achieving timing closure during physical implementation was the "useful skew" analysis feature in the Cadence SoC Encounter environment, which provided the team with advanced techniques to achieve timing on critical blocks. "Although we were accessing some advanced features in the Encounter platform, we found that it was a fairly intuitive process, and we were able to ramp up quickly," said Raghavan. "The

fact that it fit into our existing design flow and supported TSMC libraries and rules were also big time savers."

INPHI OVERCOMES FLOORPLANNING AND ROUTING CHALLENGES USING THE SOC ENCOUNTER SYSTEM

Inphi also used the SoC Encounter system's flip-chip router for automatic redistribution-layer (RDL) routing. This allowed the team to explore the impact of their implementation choices on their chip performance. "Dealing with the complexity of a mixed-signal design in a flip-chip package was nontrivial," continued Raghavan. "The automatic RDL routing was very powerful, and helped keep us on track with our schedule."

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