



CADENCE AND F5 NETWORKS, INC.

F5 Networks Saves 25% on Power and 12% on Area Using Cadence Encounter RTL Compiler

“By switching to Encounter RTL Compiler global synthesis we were able to reduce power to meet our IR drop targets. We were also able to cut our random logic, which reduced area. Using Encounter RTL Compiler for synthesis provided a much better starting point for physical implementation, helping us meet our goals.”

Al Danielson, Senior ASIC Engineer, F5 Networks, Inc.

CORPORATE PROFILE

- F5 Networks is a global leader in application traffic management

DESIGN CHALLENGE

- Design an ASIC that was approximately four times larger than previous designs in both silicon area and gate count
- Apply new methodology to deal with challenges brought on by increased design size and complexity

CADENCE SOLUTION

- Implemented Cadence Encounter® RTL Compiler global synthesis

CADENCE PRODUCTS AND SERVICES

- Cadence Encounter digital IC design platform

SAFE, RELIABLE, AND AGILE APPLICATION TRAFFIC MANAGEMENT

When you think “firewall” and “security,” the next words that come to mind are probably not “accessible” or “flexible.” Enter Seattle, Washington-based F5 Networks, Inc., a pioneer and global leader in application traffic management. F5 solutions are designed to provide organizations with reliable, secure, efficient access to corporate applications from anywhere in the world, increasing productivity and flexibility for any user accessing any application in the system. By optimizing the performance of the overall system using F5 technology, organizations can increase their productivity and reduce their cost of doing business, all while keeping their data secure.

The F5 design team was embarking on a new ASIC that would test the limits of their existing design flow. “This new ASIC was close to four times larger than our previous designs in both silicon area and gate

count, including 121 SRAM instances” said Al Danielson, Senior ASIC Engineer, F5 Networks. “This increase in size and complexity severely strained our existing methodology, requiring us to explore new tools and techniques to achieve our design and quality of silicon goals.”

POWER AND GATE COUNT KEY CONCERNS FOR NEW DESIGN

The F5 team worked with Cadence to address the design challenges that F5 was experiencing. “The most significant problem we had was power,” continued Danielson. “The chip used a pad ring, and was too big and consumed too much power for us to keep a reasonable IR drop to the center of the core. We ran through many iterations of power grid design to improve the IR drop, but none solved the problem. Every spare pin on the package was used for power/gnd pairs. We needed to use clock gating and reduce the gate count to get the core power consumption down by at least 20%.”

"The problems we were facing in our new design, specifically IR drop and congestion, are traditionally thought of as issues to be solved only during physical design. Encounter RTL Compiler created a better netlist up front, so we did not have to do so much fixing during physical implementation."

Al Danielson, Senior ASIC Engineer, F5 Networks, Inc.

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CADENCE SYNTHESIS SOLUTION PROVES CRUCIAL TO F5 DESIGN SUCCESS

By working with Cadence to address some critical design concerns up front in the process, the F5 design team achieved all of their design and quality of silicon goals. "By switching to Encounter RTL Compiler global synthesis we were able to reduce power to meet our IR drop targets," continued Danielson. "We were also able to cut our random logic, which reduced area. Using RTL Compiler for synthesis provided a much better starting point for physical implementation, helping us meet our goals."

F5 NETWORKS POSITIONED FOR SUCCESS

As F5 Networks makes plans for future chips, they will continue to make Encounter RTL Compiler global synthesis a key element of their design flow. "Having a partner like Cadence increases our confidence that we can overcome the design challenges that lie ahead," said Danielson. "F5 Networks will continue to innovate for the application traffic management market, and we will leverage Cadence innovations for our design flow."

The team's other major challenge was gate count. "We were starting to see routing congestion areas that were causing long router runtimes and negative slack in some critical paths that routed through the trouble spots," said Danielson. Cadence suggested that the F5 team adopt Encounter RTL Compiler global synthesis to address both of these issues as well as others that the team was facing.

ENCOUNTER RTL COMPILER GLOBAL SYNTHESIS ENABLES NEW METHODOLOGY

Moving to Encounter RTL Compiler enabled the F5 design team to abandon their existing bottom-up methodology in favor of a top-down compile approach. "Encounter RTL Compiler didn't have the hierarchical limitation that we had with traditional synthesis technology, which proved to be a major plus in helping us deal with clock gating," said Danielson. "When we ran Encounter RTL Compiler on the design, we were able to increase the gated flip-flops count to more than 100K, up from 40K."

To address the congestion issue, Encounter RTL Compiler's results again provided an improved starting point for physical implementation. "The area result was 12% smaller than our previous best result," said Danielson. The methodology change proved a significant benefit for this portion of the design. "Some of the area benefit was due to being able to synthesize top-down. We were able to make a switch to topdown because the runtime using Encounter RTL Compiler was approximately 12 hours, compared to the 22-hour runtime needed for the bottom-up approach.

The power savings from clock gating and the area savings for the Encounter RTL Compiler synthesis and optimization algorithms were enough to decrease the internal IR drop to within the design team's requirements across all process corners. The final core power was reduced by 23%, from approximately 5.75W to approximately 4.42W.

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