



CADENCE AND EPOCH

Epoch Improves Accuracy Using Cadence RF Design Methodology Kit

“The most valuable part of the kit was the five days of applicability consulting that we received from Cadence. We learned about features that we didn’t have time to look at. It was great to learn that we already had a number of pre-defined solutions in the kit that resonated with problems we were having.”

Dr. Aleksander Dec, Vice President and Co-founder, Epoch Microelectronics, Inc.

CORPORATE PROFILE

- Epoch Microelectronics, Inc. is a design house specializing in analog, RF and mixed-signal ICs for the cellular phone, satellite, and cable markets.

DESIGN CHALLENGES

- Larger chips but shorter design cycles
- Integrating an entire transceiver supporting multiple standards onto a single SoC

CADENCE SOLUTION

- Integrated full-chip RF design and simulation methodology
- Mixed-signal verification

CADENCE PRODUCTS AND SERVICES

- Cadence RF Design Methodology Kit
- Virtuoso Spectre RF Simulation Option
- Virtuoso Passive Component Designer
- Assura RF Extraction

RF DEMAND RISING

Growing competition in the handheld communications device markets has assured RF designers an even more important place in current IC development. Because these devices compete among high-turnover consumer products, constant innovation has become a life-and-death market requirement. As a result, development cycles for new chips have shrunk dramatically, while demand for new features and smaller size continues to push design to the limits.

These pressures have fueled the trend toward integrating multiple standards into a single device, at the same time that multiple devices are being integrated into SoCs. The escalating complexity of these chips, combined with their shrinking line geometries, is dramatically increasing the financial risks associated with mixed-signal chip development.

Specialized design houses of expert RF designers have filled a critical need in this high-risk area. Epoch Microelectronics, based in Tarrytown, New York, has been providing state-of-the-art services under the most diverse and complex requirements for the last nine years. “Getting RF right the first time is challenging. It’s what we are striving for daily,” says Dr. Aleksander Dec, co-founder of Epoch Microelectronics.

One of the most demanding realities of this work is the need to constantly adapt to each client’s particular software design flow. Epoch engineers have been exposed to every type of design software and methodology—or lack of methodology—that exists in the market. Providing an easily integrated technology base is one way to increase the value added in the design process. When it came to investing in scalable RF design and verification solutions, Epoch chose Cadence.

CHALLENGES AND ACHIEVEMENTS

Change is the rule, not the exception. Epoch has found that because of market pressures, multiple chips for release in successive years will be developed in parallel. Later releases are undergoing constant design redefinition, while the next chip for release is on a six-month fast track to completion. “We’ve done projects where the chip was already taped out and going to mask while verification is still going on,” explained Dr. Dec.

Even in this high-pressure environment, Epoch has had many great successes, such as integrating VCOs into a complex GSM transceiver chip on a tight deadline, and completing a 10GHz VCO load block for Renesas Technology within four months. What’s more, both of these difficult projects were completed with first-silicon success.

Being on-call experts can create unique issues as well. For some projects, Epoch’s desired design and verification flow cannot be used because the client’s CAD department supports a different set of tools. During VCO design in such situations, Epoch is unable to perform extractions and can only estimate parasitics. For example, on an actual project in a 1.2GHz range VCO, the silicon came back and tested at 10-20% below the specified frequency. This meant costly re-spins and delays before a sample could be provided to the client. Epoch realized it was necessary to bring a more productive engineering methodology to this type of engagement.

FEATURES THAT MAKE A DIFFERENCE

Once they adopted the Cadence® RF Design Methodology Kit and began to use the Virtuoso Passive Component Designer (VPCD) and Cadence Assura® RF—which provide full-chip simulation capability and RLCK extracted views—Epoch was able to immediately improve the frequency accuracy of VCO designs to 0.9-1.9%. This represented not only a tenfold improvement over the 10-20% range in the example above but also a huge savings in both time and cost.

Epoch’s experience with other vendors has not always been positive in this time-pressured environment. “Assura RF is much easier to work with, even if we use the complete RLCK. The file sizes are manageable and the simulation time is manageable, and yet it provides the accuracy we need,” said Dr. Dec.

Stability analysis (STB) was another pleasant surprise for Epoch. “We have been Cadence technology users for many years and are fairly proficient with Cadence solutions. However, when we installed the latest Virtuoso release, we noticed that new stability analysis functionality had been added. So we called our local Cadence application engineer, who walked us through the new functionality, and now everyone at Epoch knows how to use STB analysis. That was a real plus,” continued Dr. Dec.

The Cadence RF Design Methodology Kit includes an envelope analysis capability that also proved very useful. Epoch had designed a crystal oscillator using another solution provider’s software and was having trouble meeting the specifications. The frequency divider circuit was demonstrating strange and unpredictable convergence behavior with the third party’s harmonic balance simulator. When Epoch ran the Cadence oscillator envelope analysis, it accurately predicted the problem, allowing engineers to correct it before going to silicon.


“The real value derived from the RF Methodology Kit is in the interaction with a Cadence application engineer and optimizing our overall RF design and verification flow,” commented Dr. Dec. “Since we do not have time to explore every new functionality in the software, we usually rely on our Cadence application engineer to update us on the product enhancements by leveraging the reference design in the RF Design Methodology Kit. We also use the reference design in the kit to communicate our issues to the Cadence application engineer, who usually responds in a timely manner and shows us how our simulation and verification needs can be addressed by demonstrating the results in the reference design.”

LOOKING AHEAD

There are features in both the methodology and the kit that Epoch is still learning to implement. One of these involves using the Verilog®-A language and a top-down approach to design through verification. “If there is a bug at the circuit level, it looks like it will be easier to switch blocks in and out with Verilog-A,” said Dr. Dec.

One of the challenges Epoch faces in RF design is how to perform accurate sigma delta converter simulations in PLL circuits. “Some people will try to predict the outcome quickly by modeling the spectrum, but this is not complete; it’s kind of like cheating. We are very interested in the Cadence algorithm to simulate a sigma delta synthesizer at the transistor level,” explained Dr. Dec. “We want to be able to put imperfections into the PLL, and then look at the effect they have on the behavioral level and then on the circuit level.”

Because of this broad and growing design and verification platform, Epoch views Cadence as a significant partner in the continuing development of its own design consulting value.



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