



CADENCE AND AGERE SYSTEMS

Agere Saves Six Months in Project Schedule using Cadence
Palladium Accelerator/Emulator

“Adopting the Palladium accelerator/emulator in our design flow saved six months in our project schedule. It was a major shift for us. We were able to start software development nine months earlier than in our previous design, which allowed us to deliver both hardware and software to one of our customers just one week after the chip came back from the fab.”

Craig Garen, Vice President of Product Development, Agere Systems

CORPORATE PROFILE

- Agere Systems is a provider of semiconductors for storage, wireless data, and public and enterprise networks

DESIGN CHALLENGE

- Adopt a new verification environment to enable true hardware/software co-verification
- Speed development time for 6-million-gate Link Layer Processor

CADENCE SOLUTION

- Demonstrated the power of the Cadence Palladium® accelerator/emulator by bringing up a new verification environment in only two weeks
- Success of initial project convinced Agere to choose the Incisive Palladium II system for future designs

CADENCE PRODUCTS & SERVICES

- Cadence Palladium accelerator/emulator, part of the Incisive® functional verification platform

A “TRUEADVANTAGE” FOR WIRELINE AND WIRELESS NETWORKING

There was a day not so long ago when being connected meant that you had a cell phone. Now, you get news updates on your PDA/camera/phone, you watch HDTV, and you’re thinking about a new high-end on-line gaming system. Now, that’s connected. Along with these advancements come an enormous increase in demand for bandwidth and superior service, all at the best possible price.

The *TrueAdvantage*™ Converged Access Solutions from Agere Systems arm telecom equipment manufacturers with the tools they need to efficiently create and deliver multiple services to any network at higher performance levels and lower cost. A key element of this offering is a new processor chip called the Link Layer Processor (LLP). “The LLP is a highly integrated solution for multiservice wireline and wireless applications, and an important part of our *TrueAdvantage*

offering,” said Craig Garen, Vice President of Product Development with Agere Systems. “To meet our time-to-market window for the LLP, we needed to adopt a new verification methodology that would shorten our development time and improve our overall quality.”

LONG-TERM COLLABORATION WITH CADENCE HELPS DRIVE CHANGE IN DESIGN METHODOLOGY

The Agere telecom engineering team had worked with Cadence on other parts of their design flow, but they were new to the idea of emulation. “Adopting emulation in our design flow created a significant shift in our process that affected many design groups beyond our own,” added Garen. “Agere’s long-term relationship with Cadence gave us the confidence to move to the Palladium accelerator/emulator, and the positive results of our decision were almost immediately apparent in the LLP project.”

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PALLADIUM ACCELERATOR/ EMULATOR ENABLES TRUE HARDWARE/ SOFTWARE CO-VERIFICATION

Cadence helped the Agere team connect the Palladium accelerator/ emulator to their testers, and Cadence built a hardware/software co-verification environment for the ARM processor in the design. "With the Palladium accelerator/ emulator in our flow, we are now able to run two copies of our design in parallel," said Garen. "Having the ability to work chip verification and validation issues during the chip design process is a huge time saver."

Importantly, ramp-up time for the new methodology was minimal. The Agere telecom design team brought up their new verification environment for the LLP project in only two weeks. "We had been looking for a true hardware/ software co-verification solution for our new design," said Garen with Agere. "The Palladium accelerator/emulator provided that capability and enabled us to dramatically improve our productivity on the very first project."

AGERE TEAM IMPLEMENTS REMOTE ACCESS OF CO-VERIFICATION ENVIRONMENT

Agere needed to find a way for remote members of the company's development group to access their new hardware/ software co-verification environment. "Cadence showed us how to achieve remote access for our team in India," said Garen. "The Palladium system is optimized for team verification, allowing us to have up to 16 users at a time, from multiple remote locations."

NEW VERIFICATION METHODOLOGY MAXIMIZES EFFICIENCIES, SPEEDS TIME TO MARKET

The Agere team met its time-to-market objective for the LLP, and improved its verification process at the same time. "Adopting the Palladium accelerator/ emulator in our design flow saved six months in our project schedule," said Garen. "It was a major shift for us. We

were able to start software development nine months earlier than in our previous design, which allowed us to deliver both hardware and software to one of our customers just one week after the chip came back from the fab."

AGERE UPGRADES TO INCISIVE PALLADIUM II SYSTEM FOR FUTURE PROJECTS

Based on the success of the Link Layer Processor chip project, the Agere team decided to upgrade to the Incisive Palladium II system for their future projects. The Palladium II system includes enhanced emulation speed, capacity, density, I/Os, and team verification support.

cadence™

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