The Customer

Based in Oslo, Norway, Energy Micro, now a part of Silicon Labs, is a global provider of energy-friendly 32-bit microcontrollers (MCUs) based on the ARM® Cortex®-M processors. Silicon Labs’ EFM32 Gecko MCUs consume a quarter of the energy of competing products and are ideal for energy-sensitive applications such as smart metering, building automation, security, and portable health and fitness equipment.

The Challenge

Eirik Jorgensen, formerly the vice president of engineering at Energy Micro and now a senior design engineering manager at Silicon Labs, oversees digital and analog teams that are responsible for everything from new product specifications to implementation, verification, and tapeout. Soon after its 2007 founding, Energy Micro began evaluating electronic design automation (EDA) tools to support its analog, digital, mixed-signal, and back-end flows.

Recalled Jorgensen, “We had to create our flows from scratch. We also had very limited resources at the time. It was important for us to work with someone who had a good analog toolset, a good user interface, and a good overall user experience, to make it easier for our designers.”

The design team needed a very efficient flow, as the engineering team knew it would want to have a single platform for all of its designs. Looking at some of the leading vendors on the market, the design team found that Cadence met its criteria with its tools, reference flows, and expertise.

Business Challenge

• Ramp up the company’s product development capabilities

Design Challenges

• Create and implement efficient design flow and methodology, supported by single toolset, for development of low-energy MCUs

Cadence Solution

• Integrated mixed-signal, low-power RTL-to-signoff flow based on Cadence Assura, Encounter, Incisive, and Virtuoso platforms

Results

• Saved several months in development time for design flows
• 20 months after the start-up of the company, the first 32-bit MCU (EFM32 Gecko) was launched, consuming only a quarter of the energy of competing products
• Developed new 32-bit MCU in just 4 months, saving up to 8 months of effort due to innovative design methodology and focus on re-usability

Silicon Labs and Cadence

“When we began developing the EFM32® Gecko MCU family, we made a good selection with Cadence, which provided the tool performance we needed for the entire design flow, and services to help us develop our flow.”

Eirik Jorgensen, Sr. Design Engineering Manager, Silicon Labs
The Solution

The design team implemented an integrated mixed-signal, low-power register-transfer level (RTL) to signoff flow based on several key Cadence platforms: Assura® for physical verification; Encounter® for physical implementation, power intent verification and analysis, design synthesis, and test environment development; Incisive® for multi-language simulation; and Virtuoso® for design simulation, physical layout, analog and mixed-signal full-chip verification, and design entry. These tools are now used in the Silicon Labs environment.

Jorgensen and his team also applied various low-power design techniques, including multiple supply voltage power domains, clock gating, and power-aware simulation. The Cadence flow facilitates use of these techniques. For example, with Cadence Encounter RTL Compiler, the team could apply clock gating automatically during synthesis, and Incisive technologies support power-aware simulation in the Common Power Format (CPF).

“One of the main reasons we chose Cadence was that we wanted one vendor for all of the tools to simplify the flow and simplify support,” said Jorgensen. “This was an intense process, with no design to benchmark performance because we were starting from the ground up.

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Cadence developed a flow that allowed each designer to work independently as well as collaboratively on their sections. Focusing on low power on all stages from block design through system integration, Cadence provided thorough training for the engineers, enabling them to take advantage of the features in the different tools.

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Said Jorgensen, “We were able to focus on system specifications and start on our designs while the flow was developed. Once we began using the completed flow, we became productive very quickly thanks to the good support from Cadence.”

The Results

To date, the EFM32 Gecko design team has developed more than 250 MCUs using Cadence's comprehensive CPF-driven mixed-signal and low-power design methodology. Within just a few weeks of implementation, the team was able to have a primary flow running so the engineers could synthesize and do the schematics. Another two months later, the team had its power-aware methodology running. Cadence engineers helped to modify the flows to meet the team’s needs. Without Cadence’s support, said Jorgensen, the team would probably have needed several more months to get these flows off the ground.

“Using a single vendor’s mixed-signal flow, we were able to easily integrate our analog and digital sides while maintaining low power consumption and avoiding any incompatibility between the two different sides,” noted Jorgensen.

To highlight the efficiencies the design team has gained, Jorgensen said that it took about four months of effort for up to three engineers to complete an all-new 32-bit MCU design. For a comparable product development, such an effort would typically require up to one year of work. “It’s quite amazing to achieve this, which indicates our flow is extremely efficient,” added Jorgensen.

Summary and Future Plans

Silicon Labs, with the addition of the Energy Micro team and EFM32 product portfolio, regularly evaluates its design flows to ensure that there is unification and efficiency. Any need for new tools remains to be seen; however, the company is continuing to pursue aggressive technologies and maintains a wide range of products in its roadmap.