



## Cadence Design Systems

Cadence is a global leader in software and hardware design tools, silicon intellectual property, and design services that are transforming the electronic design automation (EDA) industry. The Cadence® vision for this transformation is called EDA360 because it embraces the entire spectrum of the design process and focuses on end-product profitability. This applications (“apps”)-driven approach to creating, integrating, and optimizing electronic designs helps our customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. Cadence is headquartered in San Jose, California, with design centers, research centers, and sales offices around the world.

### Markets and Trends

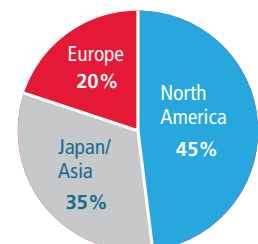
Cadence serves the \$2-trillion global electronics market, including the more than \$300-billion semiconductor market. The major vertical market segments include: wired and wireless communications; industrial, medical, and automotive electronics; computers; and consumer electronics, such as multimedia and personal entertainment devices. These segments account for more than 90 percent of electronics equipment revenue and semiconductor revenue worldwide. The main horizontal market segments are systems companies, semiconductor companies, and silicon providers (ASIC vendors, IC foundries, and FPGA companies). As a leading provider of EDA solutions in these segments, Cadence has unparalleled insight into industry trends and customer needs.

Two major trends drive electronics design: ever-increasing silicon capacity and escalating complexity. Although traditional manufacturing methods are reaching the fundamental limits of physics, silicon capacity will continue to grow as

### Corporate Facts

Founded	1988
Corporate Headquarters	2655 Seely Ave, San Jose CA 95134 USA
Worldwide Locations	<a href="http://www.cadence.com">www.cadence.com</a>
NASDAQ Symbol	CDNS
Primary Business	Electronic design automation software, hardware, IP, and services

Approximate Sales by Geography in 2011



new transistor configurations are deployed and individual slices of silicon in separate packages become stacks of silicon interconnected within a single package.

Meanwhile, designs are also becoming more complex due to the convergence of design domains and to consumer demand for high-performance applications. Modern electronics devices support high-speed communication, massive data manipulation, and rapid interactivity in chips that require mixed-signal (analog/digital), low-power, and advanced-node design technologies. In many cases, a product's hardware capabilities are not the differentiator. Today's products compete mainly on the basis of the apps—the software they can run—whether they're games on a mobile phone or protocols on a network router.

To be successful, new designs must be optimized at the system level, as well as system-on-chip (SoC) and silicon levels. Cadence is the only company with the combination of industry vision, product line breadth, and advanced technology to fully address all of these challenges.

### Cadence EDA360 Solutions

Cadence product development is driven by the EDA360 vision, which expands the traditional hardware-only focus of EDA to include the development of complete hardware/software platforms ready for applications deployment. EDA360 defines three levels of design: Silicon Realization, SoC Realization, and System Realization.

#### Silicon Realization

Silicon Realization encompasses everything it takes to get a design into packaged silicon. The end result could be analog, digital, or mixed-signal intellectual property (IP) for SoC integration; a complete IP subsystem; or an entire integrated circuit (IC)—a chip—without embedded software. Silicon Realization requires tools and IP that enable the design, verification, and implementation of complex designs across silicon, package, and board.

Cadence delivers end-to-end Silicon Realization flows that build upon our strong base of proven technologies, methodologies, and design and methodology services. Thousands of engineers worldwide use our solutions daily to overcome the key Silicon Realization challenges like low-power, mixed-signal, high-performance design; enterprise verification for large, complex chips; and advanced packaging techniques like 3D-IC and system in package.

#### Custom and Analog Design

The Cadence Virtuoso® unified custom/analog flow supports designs that must be developed at the transistor level for maximum performance, including analog and RF circuitry, high-performance digital blocks, and the standard cell libraries used as building blocks for digital ICs. Virtuoso technology supports design entry, simulation, generation of physical layouts, and verification—ultimately driving the equipment that manufactures ICs. Virtuoso technology can also be used in conjunction with

### Financial Highlights

(In thousands, except per share amounts)

	2011	2010	2009
Revenue	\$1,149,835	\$935,954	\$852,632
Net income (loss)	\$72,229	\$126,538	(\$149,871)
Net income (loss) per share, assuming dilution	\$.27	\$.48	(\$.58)
Cash, cash equivalents, and short-term investments	\$604,639	\$570,124	\$571,299
Total assets	\$1,761,269	\$1,732,116	\$1,410,587
Stockholders equity	\$411,130	\$276,654	\$108,373

\* Adjusted for the retrospective adoption of new accounting principles as required by the "Debt with Conversion and Other Options" subtopic of the FASB Accounting Standards Codification.

our Encounter® unified digital flow to provide the industry's most comprehensive mixed-signal design, implementation, and verification offering.

#### Digital Design

The Cadence Encounter unified digital flow converts high-level descriptions of a digital IC into physical implementations, performs placement and routing, and provides parasitic extraction and analysis tools that optimize and verify timing and power requirements. Encounter technology incorporates design-for-manufacturing (DFM) capabilities that ensure an IC can be manufactured successfully with high yields. The data produced by Encounter technology can be used to create photomasks for chip manufacturing.

#### Enterprise Verification

It's often more difficult to verify the correctness of the logical design of an IC than to design it in the first place. Cadence Incisive® technology delivers fast and efficient metric-driven verification, which uses an executable verification plan to measure and track progress. Incisive tools support both simulation (test cases generated either randomly or directly) and formal verification (exhaustive mathematical proofs). Incisive technology natively verifies low-power designs, links tightly to Virtuoso analog/mixed-signal verification, works efficiently with Cadence Verification IP, and integrates with the Cadence System Development Suite for acceleration, emulation, and hardware/software co-verification, providing a complete verification solution.

#### Package and PCB Design

Silicon die must be packaged and mounted on a printed circuit board (PCB). Cadence Allegro® system interconnect and system-in-package (SiP) technologies support IC/package co-design, which concurrently optimizes both the silicon die and the package in which it sits. Allegro tools provide a comprehensive PCB design, analysis, and physical layout solution.

## SoC Realization

SoC Realization refers to the design of a system on chip (SoC), which incorporates one or more processing elements and interfaces plus memory. Cadence SoC Realization offerings include design intellectual property (IP), services, and tools and methodologies for the architectural exploration, integration, verification, and implementation of complex SoCs.

Modern SoCs consist of reusable silicon IP blocks—often acquired from outside sources—that are then combined into subsystems for compute, memory and storage, and interface subsystems. Compute and interface IP requirements are well established and widely understood. Meanwhile, the challenges surrounding memory and storage are growing as the data demands on multi-core SoCs increase. This, in turn, drives the need for the most advanced SoC design and implementation capabilities.

Cadence provides differentiated, integrated, and proven design IP and services for memory and storage management and for interface protocols, enabling customers to develop innovative and competitive products. Cadence also provides a comprehensive verification IP (VIP) catalog that greatly eases the development of functional verification environments. With a 10-year legacy of production-proven VIP, Cadence offers the industry's broadest portfolio with support for 30+ complex protocols and more than 15,000 memory devices.

## System Realization

System Realization is the development of complete hardware/software (HW/SW) platforms that provide all necessary support for end-user applications. It includes the architecture, design, integration, and verification of complex systems, as well as the required HW/SW infrastructure.

Because apps have become the primary product differentiator, systems companies now expect semiconductor companies to provide not just silicon, but complete HW/SW systems ready for apps deployment.

The Cadence System Development Suite was introduced to help customers address these challenges with a set of four platforms for concurrent hardware/software design and verification, accelerating system integration, validation, and bring-up time. The suite features the Rapid Prototyping Platform, Virtual System Platform, Palladium® XP Verification Computing Platform, and Incisive Verification Platform. Supporting industry standards and multiple levels of design abstraction, the suite allows for easy migration among platforms and between HW/SW domains, and can scale to meet performance, capacity, and software distribution volume needs as they change.

Successful System Realization also requires faster turnaround time for the development and reuse of complex designs. Using the Cadence transaction-level modeling (TLM) design flow (which includes high-level synthesis from Cadence C-to-Silicon Compiler), many leading semiconductor and systems companies are tackling the challenges of today's intricate system designs.

Finally, verifying that memory interfaces and other protocol interfaces perform correctly is crucial to System Realization. Cadence memory models and extensive protocol support enable engineers to analyze system-level data transactions during simulation, which simplifies the verification process, reduces risk, and increases confidence in the final product quality.

## Services

Cadence provides engineering services to help semiconductor and systems companies design complex ICs, implement key design capabilities, and adopt new methodologies without the risk. By assisting customers from product concept to volume manufacturing, and by leveraging our experience and knowledge of design techniques, Cadence Services can boost the productivity of our customers' engineering teams.

## Executive Team

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Senior Vice President and  
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