About Us

Cadence is a leading provider of electronic design automation (EDA) and semiconductor intellectual property (IP). Our custom/analog tools help engineers design the transistors, standard cells, and IP blocks that make up systems on chip (SoCs). Our digital tools automate the design and verification of giga-scale, giga-hertz SoCs at the latest semiconductor processing nodes. Our IC packaging and PCB tools permit the design of complete boards and subsystems.

Cadence also offers a growing portfolio of design IP and verification IP for memories, interface protocols, analog/mixed-signal components, and specialized processors. And at the systems level, Cadence offers an integrated suite of hardware/software co-development platforms. In short, Cadence’s innovative technologies are essential to building great products that transform lives.

Corporate Facts

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<th>Founded</th>
<th>1988</th>
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| Corporate Headquarters | 2655 Seely Ave.  
San Jose, CA 95134  
USA                  |
| Worldwide Locations    | www.cadence.com            |
| NASDAQ Symbol        | CDNS                      |
| Primary Business     | Electronic design automation software, hardware, IP, and services |
Executive Management

Lip-Bu Tan
President and
Chief Executive Officer

Geoff Ribar
Senior Vice President and
Chief Financial Officer

Tom Beckley
Senior Vice President, Custom IC & PCB Group

James J. Cowie
Senior Vice President, General Counsel and Secretary

Anirudh Devgan, Ph.D.
Senior Vice President, Digital & Signoff Group

Chi-Ping Hsu, Ph.D.
Senior Vice President, Chief Strategy Officer, EDA

Charlie Huang, Ph.D.
Executive Vice President, Worldwide Field Operations and System & Verification Group

Christina R. Jones
Senior Vice President, Global Human Resources

Martin Lund
Senior Vice President, IP Group

Nimish Modi
Senior Vice President, Marketing & Business Development

What We Offer

Custom and Analog Design
The Cadence Virtuoso® unified custom/analog flow supports designs that must be developed at the transistor level for maximum performance, including analog and RF circuitry, high-performance digital blocks, and the standard cell libraries used as building blocks for digital ICs.

Digital Design
The Cadence digital implementation flow, including Innovus™ and Encounter® technologies, eliminates iterations without sacrificing design quality by addressing timing sensitivity, leakage power, and yield variation from the start.

Signoff
To eliminate the bottleneck that timing signoff can be, Cadence offers its Tempus™ Timing Signoff Solution. With the Tempus solution, design engineers can achieve faster tapeout with a shorter timing signoff closure and analysis process. For faster power integrity and analysis signoff, Cadence offers the Voltus™ IC Power Integrity Solution.

Enterprise Verification
It’s often more difficult to verify the correctness of the logical design of an IC than to design it in the first place. Cadence Incisive® technology delivers fast and efficient metric-driven verification, which uses an executable verification plan to measure and track progress. Incisive tools support both simulation (test cases generated either randomly or directly) and formal verification (exhaustive mathematical proofs).

Financial Highlights
(In thousands, except per share amounts)

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<th>2014</th>
<th>2013</th>
<th>2012</th>
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<tbody>
<tr>
<td>Revenue</td>
<td>$1,580,932</td>
<td>$1,460,116</td>
<td>$1,326,424</td>
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<tr>
<td>Net income (loss)</td>
<td>$158,898</td>
<td>$164,243</td>
<td>$439,948</td>
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<tr>
<td>Net income (loss) per share, assuming dilution</td>
<td>$0.52</td>
<td>$0.56</td>
<td>$1.57</td>
</tr>
<tr>
<td>Cash, cash equivalents, and short-term investments</td>
<td>$1,022,606</td>
<td>$633,048</td>
<td>$827,061</td>
</tr>
<tr>
<td>Total assets</td>
<td>$3,209,556</td>
<td>$2,428,601</td>
<td>$2,287,003</td>
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<tr>
<td>Stockholders equity</td>
<td>$1,333,574</td>
<td>$1,156,105</td>
<td>$915,171</td>
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* Adjusted for the retrospective adoption of new accounting principles as required by the “Debt with Conversion and Other Options” subtopic of the FASB Accounting Standards Codification.

System Development and Verification
Systems companies now expect semiconductor companies to provide not just silicon, but complete hardware/software systems ready for apps deployment. The Cadence System Development Suite was introduced to help customers address these challenges with a set of four platforms for concurrent hardware/software design and verification, accelerating system integration, validation, and bring-up time. The suite features the Rapid Prototyping Platform, Virtual System Platform, Palladium™ XP Verification Computing Platform, and Incisive Verification Platform.

Package and PCB Design Signal Integrity/Power Integrity Analysis
Cadence Allegro® system interconnect and system-in-package (SiP) technologies support IC/package co-design, which concurrently optimizes both the silicon die and the package in which it sits. Allegro tools provide a comprehensive PCB design, analysis, and physical layout solution. Cadence OrCAD® PCB design solutions are cost effective, scalable, and feature rich, while Cadence Sigirity™ technology provides the only proven path for system-level, power-aware signal integrity/simultaneous switching noise (SSN) compliance.

IP
Cadence provides differentiated, integrated, and proven design IP and services for memory and storage management and for interface protocols, enabling customers to develop innovative and competitive products. Cadence also provides a comprehensive verification IP (VIP) catalog that greatly eases the development of functional verification environments, as well as dataplane processing units (DPUs) and digital signal processors (DSPs) for data-intensive tasks like audio, video, and image processing.

Services
Cadence provides engineering services to help semiconductor and systems companies design complex ICs, implement key design capabilities, and adopt new methodologies without the risk.

For More Information
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Media Relations: +1.408.914.6884