Trends and Technologies in Electronics

Cadence Design Systems, Inc.
February 5, 2015
Safe Harbor Statement

The following discussion contains forward looking statements, and our actual results may differ materially from those expectations discussed here.

Additional information concerning factors that could cause such a difference can be found in our Form 10-Q for the quarter ended September 27, 2014, our Form 10-K for the year ended December 28, 2013, the company’s future filings with the Securities and Exchange Commission and the cautionary statements regarding forward-looking statements in our February 4, 2015 earnings press release for the quarter ended January 3, 2015.

Regulation G

In addition to financial results prepared in accordance with Generally Accepted Accounting Principles, or GAAP, this presentation will also contain certain non-GAAP financial measures. Cadence management believes that in addition to using GAAP results in evaluating our business, it can also be useful to measure results using certain non-GAAP financial measures. Investors and potential investors are encouraged to review the reconciliation of non-GAAP financial measures with their most direct comparable GAAP financial results, including those set forth in our February 4, 2015 press release for the quarter ended January 3, 2015, which can be found in the quarterly earnings section of the investor relations portion of our website at cadence.com.
Cadence

Global leader in electronic design automation
Our products are used to design electronic products like semiconductors, mobile devices, and “cloud” infrastructure

Revenue ($ millions)

2009 2010 2011 2012 2013 2014

2014 Results

- 8% revenue growth
- 25% non-GAAP operating margin
- $317M operating cash flow

© 2015 Cadence Design Systems, Inc. All rights reserved worldwide.
Big trends creating opportunities

- **Wearable computing**: $19B Market by 2018
- **The internet of things**: $290B market by 2017
- **Cloud & Big Data**: 3.3 ZB traffic with 25% CAGR
- **Social**: 1B users on Facebook
- **Mobile**: 100M+ Tablets / year

Sources: cisco.com, gartner.com, marketsandmarkets.com, datacenterknowledge.com
Many of the opportunities are systems of systems
Smartphone is a system of systems

- Navigation
- Communications
- Photography
- Recording
- Music
- Gaming
- Productivity
Automotive vehicle is system of systems

Airbag deployment
Adaptive front lighting
Adaptive cruise control
Head-up display
Parental controls
Engine control
Automatic braking
Night vision
Windshield wiper control
Electric power steering
Electronic throttle control
Electronic valve timing
Idle stop/start
Cylinder de-activation
Active vibration control
Blindspot detection
Remote keyless entry
Parking system
Antilock braking
Transmission control
Seat position control
OBDII

Driver alertness monitoring
Accident recorder
Instrument cluster
Auto-dimming mirror
Interior lighting
Active cabin noise suppression
Voice/data communications
Cabin environmental controls
Entertainment system
Battery management
Lane correction
Electronic toll collection
Digital turn signals
Navigation system
Security system
Active exhaust noise suppression
Active suspension
Hill-hold control
Regenerative braking
Tire pressure monitoring
Lane departure warning
Electronic stability control
Active yaw control
DSRC

Courtesy: Clemson Vehicular Electronics Laboratory
Internet of things

System of systems
  ... of systems
  ... of systems
  ... of systems
  ... of systems
  ... of systems
  ... of systems
  ... of systems
  ... of systems
Diverse design requirements for IoT devices

Device Type

- **“Dumb” device**
  - Single end point
  - Single wireless standard
- **“Intelligent” device**
  - Single or multiple comms standards
- **Device or gateway portal**
  - Multiple comms standard

Requirements

- **“Dumb” device**
  - Ultra low power
  - Mixed signal
  - Very low cost
- **“Intelligent” device**
  - Multi-standard
  - High data rate
  - Flexibility
  - Low cost
  - Low power
  - Intelligence
- **Device or gateway portal**
  - Ultra low power
  - Mixed signal
  - Very low cost
Development challenges in systems of systems design require System Design Enablement
Systems of systems face development challenges from all directions
System Design Enablement
From end product down to chip level

- **CHIP** (Core EDA)
  - Design and implementation
  - IP/SoC verification
  - On-chip protocol IP
  - Dataplane unit IP
  - Software drivers

- **PACKAGE and BOARD**
  - PCB design
  - Package design
  - PCB and package analysis
  - Chip-to-chip protocol IP

- **SYSTEM INTEGRATION**
  - System analysis
  - Hardware-Software verification
  - System-level IP protocols
  - Software applications
  - Software development

- **Partnerships with Ecosystem Leaders**
  - Mobile
  - Consumer
  - Cloud Datacenter
  - Auto
  - Medical

© 2015 Cadence Design Systems, Inc. All rights reserved worldwide.
End-to-End Solutions Portfolio for SDE

Cadence Products

- Incisive® verification platform
- Allegro® package and PCB design, OrCad® PCB design
- Cadence Design IP and Verification IP
- Virtuoso® analog, custom, RF, mixed-signal design platform
- System Design with Palladium® Hybrid, Virtual System Platform
- Encounter® digital design platform
- Virtuoso® analog, custom, RF, mixed-signal design platform

System Design Enablement (SDE)

- Mobile
- Consumer
- Cloud Datacenter
- Auto
- Medical
- Others

SYSTEM INTEGRATION

PACKAGE and BOARD

CHIP (Core EDA)
Digital & Signoff: Innovative new products for advanced node leadership

Speeds timing and power analysis and verification for large, complex designs

**Quantus™ QRC Extraction Solution**
- Up to 5X faster performance
- Best-in-its-class FinFET accuracy against TSMC golden data
- Integrated into Encounter® and Virtuoso® design platforms
  - Fully certified for TSMC 16nm FinFET

**Tempus™ Timing Signoff Solution**
- 10X reduction in closure time
- Scalable to 100s of CPUs
- Optimized data structures
- Advanced process modeling
  - Unlimited multi-mode, multi-corner capacity

**Voltus™ IC Power Integrity Solution**
- Industry’s only transistor-level power integrity solution fully integrated in Virtuoso®
- Tight integration with Spectre® APS/XPS and Quantus QRC extraction
- Foundry-certified, SPICE-accurate
  - Seamless flow for full-chip, SoC power integrity analysis and signoff
  - High performance for up to a billion instances
Cadence Mixed-Signal Verification Solution ensures functionality, performance, and reliability

- **UVM – Mixed-Signal**
- Low-power intent
- Verification management
- Real-number models

- **Analog**
  - SPICE simulation
  - Spectre®
  - Spectre® APS
  - Spectre® XPS

- **Mixed-Signal**
  - Co-simulation
  - AMS Designer
  - Spectre® XPS for mixed-signal applications

- **Digital**
  - Functional verification
  - Incisive® Enterprise Simulator

**Spectre® XPS (eXtensive Partitioning Simulator) FastSPICE**
Breakthrough partitioning technology reduces simulation time from days to hours
- Easy to adopt – uses Spectre PDKs and models
- Integrated into the Virtuoso® Analog Design Environment
ARM-BASED SYSTEM VERIFICATION
LOW-POWER VERIFICATION
MIXED-SIGNAL VERIFICATION
FUNCTIONAL SAFETY
Hybrid verification technology for embedded SW development

Start software validation up to 6 months earlier

Boot the OS 60 X faster with Palladium® hybrid mode
Comprehensive SoC IP solution
Silicon-proven, customer-verified

VIP support for all major protocols and memory models

Customizable IP

HW/SW optimized

Digital and analog dataplane processing

More complete SoC IP portfolio

Memory and Storage IP
Interface IP
AMS/Analog IP
Peripheral IP
Processing IP
Advanced tools for PCB and IC packaging
OrCad and Allegro design suites, Sigrity analysis

PCB
Front-to-back flow – design, verification, analysis, and compliance closure for gigabit design challenges

3D-IC
Chip/package co-design for 2.5D- and 3D-IC
TSMC Reference Flow 12.0

Sigrity
Signal integrity, power integrity, and thermal analysis
System, PCB and IC package
New technology requires closer collaboration – from IP through manufacturing
Financials
Recurring revenue model
Visible revenue stream

90%+ recurring revenue model
• Visible and predictable software revenue stream
• ~90% of projected quarterly revenue from backlog
• Average term: 2.4 - 2.6 years

Backlog (Q4'14): $2.1 billion
Cash flow, capital structure, and uses of cash

Cash flow
- 2014: $317m

Capital structure (Q4’14)
- Cash: $1.02b
- Share repurchase: ~$38m
- Senior unsecured notes: $350m*
- Convertible debt: $350m
- Credit facility: $250m (undrawn)

Capital allocation
- Organic investment
- Retire convertible debt
  - $350m - June 2015
- M&A
- Repurchase stock

* Senior unsecured notes issued October 9, 2014.
Cadence opportunity

Dynamic electronics industry creates opportunity for growth

System Design Enablement - Complete solutions, from silicon to system

Industry leader with culture of innovation

High-visibility subscription business model