

# Virtuoso Analog Design Environment GXL

Built-in parasitic estimation and yield optimization for system-level simulation and analysis

Cadence® Virtuoso® Analog Design Environment GXL provides all the capabilities of Analog Design Environment L and XL for thorough exploration and validation of a design. Additionally, Virtuoso Analog Design Environment GXL enables users to explore parasitic effects and sensitivities to improve yield; create design-specific corners and behavioral models for accurate system-level simulation; and find the optimum design over nominal, corner, or target yield. A flexible licensing methodology further ensures a cost-effective application of GXL capabilities.

## Virtuoso Analog Design Environment

The Virtuoso Analog Design Environment product suite provides all the capabilities required to fully explore, analyze, and verify a design against the user's desired goals, allowing designers to maintain design intent throughout the design cycle. As the industry's leading solution for analog simulation control and management, it allows users to flexibly select the tier that best supports their design goals as they move through the design flow. Analog Design Environment L provides a quick entry into the analysis process with easy execution of simulations. Analog Design Environment XL extends the L tier capabilities, providing multiple test support, analysis over sweeps, corners, and Monte Carlo; easy reviewing of all results directly; and generating spec-comparison sheets and datasheets as needed. Analog Design Environment GXL builds on L and XL capabilities by providing targeted tools that aid with key design challenges with early parasitic analysis, design centering, and designing in multi-technologies.

## Virtuoso Analog Design Environment GXL Overview

Virtuoso Analog Design Environment GXL uses the same advanced design and simulation cockpit as Analog Design Environment XL and includes extended analysis capabilities for more detailed design exploration. A user can choose to launch Analog Design Environment GXL directly or just access the additional analysis capabilities from Analog Design Environment XL.

### Benefits

- Extended design exploration with sensitivity and mismatch analysis
- Advanced optimization algorithms improve design centering and yield
- Built-in parasitic estimation flow helps design convergence by making it possible to quickly identify and analyze parasitic sensitivities prior to layout
- Support for multiple technologies to facilitate multi-chip design analysis
- Generate corners specific to your design

- Model calibration and validation support for Verilog® A and Verilog AMS languages
- Supports design abstraction by providing the ability to generate Liberty and Wreal models from simulation results for system-level simulation

### Features

#### Extended analysis

To further understand the behavior of a design, users can run Sensitivity analysis to identify weaknesses in a design to process variations and for design sizing. Users can then automatically create design specific corners for signoff-level simulation.

Built upon the statistical analysis capabilities in Analog Design Environment XL, Mismatch analysis can be used to further explore the sensitivities of a design for all or a selected set of devices.

For designs where high-yield margin is critical, such as memory, a high-yield analysis capability provides up to six-sigma accuracy, without the cost of running extensive Monte Carlo.

## Parasitic resimulation

Users can explore parasitic effects early in the design flow with the ability to assign parasitic estimates onto nets and ports of their design, without editing the schematic. An estimated view is compiled for simulation across all the tests and analysis options available in Analog Design Environment XL or GXL to identify areas to focus on in the design development. Similarly, post-layout extracted designs can also be submitted for validation against the design goals or compared against the original parasitic estimates. Parasitic effects can be easily copied from an extracted view back to an estimated view to gain full access to all the debug capabilities Analog Design Environment GXL.

## Design centering

With the set-up of tests and specifications already available in Analog Design Environment XL, users can simply add the ranges of devices they want to explore and use Analog Design Environment GXL optimization engines to find the optimum design. With an array of local and global optimization choices available, the user can control how the optimizer runs to center a design over nominal, all defined corners and with parasitic estimates in place.

## Design for yield

Designers can use a series of both global and local optimization methods to center their design values to help maximize yield. For circuits requiring high design margins up to six-sigma, the internal design goals are tightened as it optimizes the parametric yield.

## Design characterization and modeling

A number of modeling options are available. Using a template-based methodology, a user can generate all the testbenches needed to explore a design and extract the parametric data needed to build a calibrated model. Model languages supported are Verilog A and Verilog AMS with full calibration, while users can also create models from parametric data in Verilog D, Liberty, and Wreal model formats.

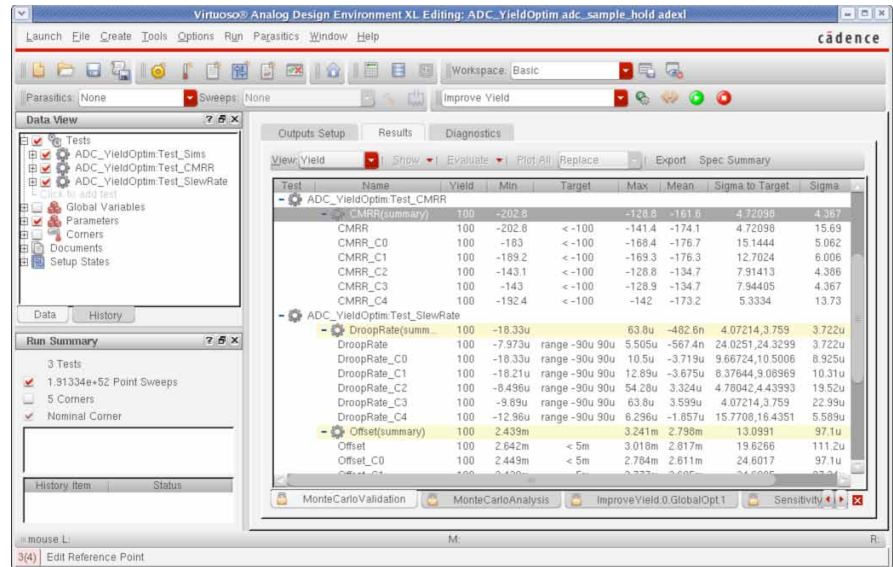


Figure 1: Virtuoso Analog Design Environment GXL: Extends analysis into parasitics and yield

## Multi-technology support

Technology support is available to aid in the design of complex multi-chip solutions, and integrate them into a single package in conjunction with the Cadence Allegro® system interconnect design platform.

## Specifications

### Extended analyses

- Inherits all features and functionality from Virtuoso Analog Design Environment XL
- Sensitivity analysis on design parameters, statistical parameters, and design variables
- Mismatch analyses
- Generate design-specific corners
- High-yield measurement
- Calibrate behavioral models for more accurate system-level simulation
- Import simulation results to build Liberty models without prior knowledge of the language
- Multiple technology support with Allegro platform to enable System-in-package (SiP) design

## Parasitic analysis

- Supports exploration of design parasitic effects before layout
- Adds R, L, C, or K parasitic elements without altering the schematic
- Full simulation support of post-extracted layouts
- Compare pre- and post-layout parasitic effects

## Optimization options

- Four local and global algorithm choices
- Optimize nominally or over corners, with or without parasitic estimates
- Run optimization with or without a starting point
- Improves design yield and design centering up to six-sigma margins

## Third-party support

Interface support for all commercial circuit simulators, including Synopsys Hspice, Mentor Graphics Eldo, Silvaco SmartSpice, and Agilent ADS. In addition, users can integrate their own proprietary circuit simulator.

## Design inputs

- OpenAccess data objects
- Cadence proprietary languages: OCEAN and MDL
- SPICE netlists
- Circuit design language (CDL)
- SPICE
- VHDL IEEE 1076-1993
- Verilog® IEEE1364
- SKILL
- PSF and PSF XL waveform formats
- SST2 waveform format
- Cadence SKILL

## Design outputs

- XML database
- PSF and PSF XL
- SST2
- Comma Separate Value
- Cadence proprietary script language: OCEAN

## Platform/OS

- X86 Linux
- Sun Solaris
- IBM AIX



Figure 2: Sensitivity of device parameters to measured goals

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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