

Virtuoso Digital Implementation

Automatic digital block implementation for a mixed-signal design methodology

Cadence® Virtuoso® Digital Implementation is a complete and automatic synthesis/place-and-route system. It enables capacity-limited block implementation for small digital components in the context of an advanced analog-driven mixed-signal design. Driven by unified design intent and abstraction, and powered by OpenAccess interoperability, Virtuoso Digital Implementation ensures a consistent and convergent design flow that accelerates time to market for complex mixed-signal designs.

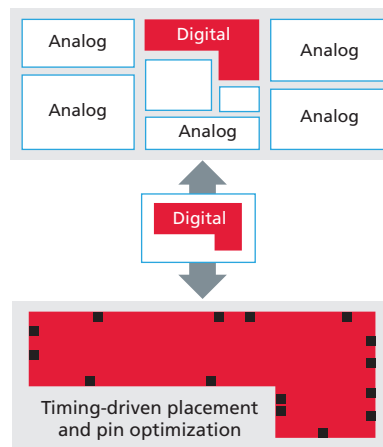
Virtuoso Digital Implementation

Virtuoso Digital Implementation delivers a capacity-limited¹, automatic, RTL-to-GDSII implementation solution for small digital blocks that complements an analog-driven mixed-signal design methodology with the Virtuoso platform. Virtuoso Digital Implementation leverages Cadence Encounter® RTL Compiler for physical synthesis and Encounter Digital Implementation System functionality for physical implementation. Used in combination, these technologies speed turnaround time from synthesis to optimization to verification, and deliver high-quality, high-performance, and lower-power digital blocks for mixed-signal designs.

Benefits

- Rapid design closure and shorter overall design cycle
 - Timing-driven implementation uses a common (Encounter) timing engine and a signoff-quality delay calculator

Mixed-signal integration at the top level in the Virtuoso environment



Digital block implementation in the Encounter environment

Figure 1: Virtuoso Digital Implementation for smaller digital block implementation in a mixed-signal design

- Faster convergence on design goals and fewer iterations
 - Concurrent design and optimization of timing, area, and power minimizes and eliminates late-stage unwanted surprises

- Unified design intent and abstraction through integration with the Virtuoso platform ensures consistent design constraints throughout the entire flow²
- Co-design of digital and analog components in a single environment
 - Built-in OpenAccess interoperability enables fast and precise top-level integration
- Rapid timing convergence for mixed-signal blocks
 - Ensures accurate static timing analysis of all digital logic paths using full-timing models and physical optimization
- Integrated power planning, power routing, and what-if power analysis enables smart power rail synthesis
- Support for multiple power domains enables a low-power methodology
- State-of-the-art clock tree synthesis
 - Optimizes clock gating for low-power designs; supports multiple and re-convergent clocks
- Advanced node design-enabled
 - Supports libraries and rules for multiple process technologies down to 28nm

¹ Virtuoso Digital Implementation is an RTL-to-GDSII solution for capability-limited designs of 50K instances or less. Please refer to the License Document for licensing details.

² Requires Virtuoso Layout Suite XL or Virtuoso Layout Suite GXL.

Features

RTL synthesis

- Enabled by Encounter Digital Implementation System L
- Read/write standard inputs/outputs
- Built-in high-performance data path
- Arithmetic optimizations
- Total negative slack (TNS) optimization
- Testability analysis and scan insertion
- Clock gating
- Multi-Vt leakage power optimization

Design exploration and prototyping

- Enabled by First Encounter® technology
- Full gate-level placement
- 10x faster detailed trial routing for higher correlation with final implementation
- 10x faster analysis with 2.5-D parasitic extraction
- Delay and timing analysis using industry-standard timing library and constraints formats
- Physical optimization technology for advanced timing closure
- In-place optimization for cell resizing, buffer insertion, and load splitting
 - Leakage power optimization
 - Advanced logic restructuring option

Clock tree synthesis

- Ultra high-speed clock tree synthesis to minimize clock skew and insertion delay
- Support for gated clocks and multiple clock domains
- Post-route clock tree optimization
- Useful skew analysis and optimization

Advanced power planning

- Quick power planning, including static and dynamic power consumption analysis
- Built-in power/IR drop analysis
- Fine mesh routing supported with embedded macro blocks
- Power-grid design results in IR drop numbers within 10% of SPICE
- Interface to signoff power-grid verification requires an Encounter Power System license, which must be purchased separately

Placement and routing

- LEF/DEF data transfer via standard interfaces and OpenAccess³
- Rectilinear block support
- Industry-proven routers
- Support for advanced engineering change order (ECO) routing
- Wire editor environment for custom edits

Easy to use

- Built-in signal and power wire editing functionality
- Tcl programming interface throughout the flow
- Intuitive and helpful commands
- Familiar use model
- Ramp up within a week
- Helpful reports for all steps

Specifications

Input

- HDL (to synthesis): Verilog, VHDL, SystemVerilog (directives, pragmas)
- Logical and timing library: library format (.alf), TLF, .lib

- Physical library: LEF
- Mixed-language/mixed-level netlist: gate-level netlist in Verilog, gate-level EDIF netlist
- Timing constraints: SDC
- Floorplan information: PDEF
- Detailed floorplan information: DEF
- Delay information: SDF
- Interconnect parasitics: DSPF/RSPF, SPEF

Output

- Optimized gate-level netlist (from synthesis)
- Netlist: DEF, Verilog
- Interconnect parasitics: DSPF, SPICE, SPEF
- Delay information: SDF
- Floorplan and placement: DEF, PDEF
- GDSII

Platforms

- Linux (32- and 64-bit)
- Solaris (64-bit)
- SOLX86 (64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

³ The loading/display/data handling of custom objects—including Pcells, RODs, multi-part paths, and fig groups—is enabled by the Encounter Mixed-Signal GXL Option, which must be purchased separately.