

SOC ENCOUNTER RTL-TO-GDSII SYSTEM

The Cadence® SoC Encounter™ RTL-to-GDSII System supports large-scale complex flat and hierarchical designs. It combines advanced RTL and physical synthesis, silicon virtual prototyping, automated floorplan synthesis, clock tree and clock mesh synthesis, advanced nanometer routing, mixed-signal support, advanced low-power implementation, and a complete suite of design for manufacturability, variation, and yield optimization technologies required for advanced node designs. These and other capabilities deliver the highest quality of silicon (QoS) for timing, signal integrity, area, power, and yield, including integrated statistical-based analyses and optimization.

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The SoC Encounter System combines RTL synthesis, silicon virtual prototyping, design planning, and full-chip digital implementation in a single system, and has been enhanced to support today's high-performance advanced node designs. Engineers can synthesize, physically implement, and optimize a flat virtual prototype—with the benefit of actual routed interconnect—giving designers an early, accurate view of design feasibility. Once feasibility is established, designers can immediately progress to full-scale implementation without ever having to leave the environment. The SoC Encounter System enables the utmost in manufacturing predictability and advanced timing closure using native signoff analysis engines delivering the best QoS.

BENEFITS

- Silicon-proven system handles flat and hierarchical 100M+ gate designs
- Combines the power of RTL synthesis, silicon virtual prototyping, physical synthesis, full-chip design implementation, and final signoff analysis in a single unified environment
- Dramatically increases productivity with an integrated, high-performance, high-capacity design solution to address large-scale, complex chips
- Enables rapid design exploration and accurate chip feasibility analysis, including an automated floorplan synthesis and ranking system for a flexible and predictable path to design closure
- Provides a flexible solution to address the latest low-power advanced node and mixed-signal design requirements
- Offers integrated and consistent process variation analysis and optimization, including multi-mode, multi-corner (MMMC) and statistical intra-die, die-to-die, wafer-to-wafer, and random variation support utilizing industry-standard statistical ECSM library models and characterization
- Brings significant productivity gains through signoff-driven implementation, and intuitive and visual global timing, power, and clock debug and diagnostics features
- Enables concurrent design and optimization, of chip and package with integrated automatic area and peripheral I/O placement and optimization, including RDL routing capabilities

FEATURES

MULTIPLE IMPLEMENTATION STYLES

The SoC Encounter System supports all implementation styles—from flat or hierarchical to single or multi-VDD. The system's fast automatic power grid design and optimization, global routing, in-place optimization, and global timing debug capabilities provide a robust infrastructure to implement any methodology. Full-chip flat prototyping delivers complete and accurate physical, timing, clock, and power data, thereby eliminating the guesswork associated with traditional block-based approaches.

SoC Encounter hierarchical support further helps physical designers to assess how best to partition the logical hierarchy into physical modules by analyzing the optimal pin assignments; quick time budgeting; accurately predicting the clock distribution networks; analyzing the power grids; and eventually generating complete timing and physical constraints for each of the physical modules.

ADVANCED RTL SYNTHESIS

RTL synthesis for high-performance systems requires not only high capacity but also advanced features to optimize the design. The SoC Encounter System supports register retiming, accurate physical layout prediction, multi-supply voltage (MSV)-aware synthesis, and other features to achieve high quality of silicon. In addition, high capacity has been given special emphasis through multithreading support.

AUTOMATIC FLOORPLAN SYNTHESIS AND RANKING

Today's physical design teams are expected to start physical implementation and design planning very early in the design cycle—with early and multiple versions of the design netlist—to determine design feasibility. Among the questions needing answers are the following: Can the design be

implemented in the required area? Can the design operate at the desired speed? Does it meet power requirements?

The production-proven automated floorplan synthesis of the SoC Encounter System closes the gap between the architecture and implementation by enabling timing-, power-, area-, and congestion-aware placement coupled with fast global routing and in-place optimization. These features enable designers to quickly generate prototype floorplans.

Add to this the built-in flexibility and editing capabilities such as relative floorplanning—specifying relationships for pre-routes, resizable objects, multiple relations, datapath stacking, and integrated analysis tools—and the designers are now able to quickly and accurately reach an optimal final floorplan.

Additionally, the floorplan ranking system helps designers to automatically generate multiple floorplan scenarios in parallel and analyze them based on predefined quality-of-results (QoR) criteria to explore as much of the physical solution space as possible and to enable the most informed assessment of design feasibility.

ADVANCED DESIGN CLOSURE

The global physical synthesis capability of the SoC Encounter System optimizes multiple paths simultaneously while performing multi-dimensional and concurrent optimization for timing, signal integrity (SI), power, area, congestion, and wire length and yield, using native signoff engines in the process. Additionally, significant improvements in performance, accuracy, and throughput can be achieved using robust MMMC analysis and optimization technologies.

NANOMETER ROUTING

With its patented architecture and fast concurrent S.M.A.R.T. routing technology (unified signal integrity, manufacturing-aware, routability, and

timing optimization), litho-aware routing, and the industry's only superthreading technology, Cadence NanoRoute® Router is unmatched in quality and performance for block-level and top-level routing, while simultaneously meeting multiple design objectives for the ultimate DRC-clean tapeout-ready GDSII database.

The NanoRoute Router further extends its leading gridded and graph-based routing and optimization technologies to include space-based technologies and support for the latest 65- and 45-nanometer design rules. Space-based route optimization becomes especially important in the presence of design-for-yield requirements, where having the flexibility to go beyond the routing grid can provide significant yield improvements not achievable in any other system. Finally, NanoRoute routing features superthreading—which combines the best of both multithreading and parallel-processing techniques—to deliver the power to route millions of nets per hour on readily available and inexpensive 32-bit computer farms.

ADVANCED PROCESS VARIATION SUPPORT

Variations in manufacturing can result in structural changes in devices and interconnect, leading to deviations in their electrical behavior. At 65 nanometers and below, process control becomes significantly more challenging, leading to a larger variation as a percentage of the total size of the design's features. As a result, designs that pass traditional signoff standards could still fail in silicon due to process variations.

In addition to providing foundry-supported signoff technologies for timing, SI, and power during implementation, the SoC Encounter System further extends these technologies by employing location-based on-chip variation (LOCV), which uses logic level and physical location to select the optimal de-rating factor. LOCV eliminates the excessive guardbanding associated with traditional de-rating and improves timing closure.

SoC Encounter technology also supplements traditional single- and multi-corner-based methods with powerful and accurate statistical static timing analysis (SSTA) that accurately accounts for variability of process parameters in a single run. Using advanced statistical ECSM models, the SoC Encounter System identifies cells and nets on both clock and data paths that are sensitive to variations, and determines the probability of timing failures over the full scope of the process window. This reduces pessimism and allows for less guardbanding, which decreases area and power consumption while improving chip performance. SoC Encounter SSTA capabilities also reduce design cycles by decreasing the number of required timing runs while enabling designers to tape out with confidence in achieving their timing goals in silicon.

ADVANCED GLOBAL DEBUG AND DIAGNOSTICS

Considering the growing challenges and complexities of design, the ability to debug and diagnose interdependent design closure issues has become increasingly important. The challenges often come late in the design cycle, along the critical path for reaching final tapeout.

SoC Encounter debug and diagnostics capabilities provide significant advantage by enabling designers to quickly zero in on and visualize interdependent timing, clock, and power issues, then quickly resolve them using powerful “what-if” analysis techniques—with results that can be immediately implemented in physical design.

LOW-POWER DESIGN

Advanced low-power techniques such as power gating (MTCMOS) and dynamic voltage and frequency scaling (DVFS) use multiple power domains. The underlying infrastructure of the SoC Encounter System simplifies the implementation of these designs because it is multiple-power-domain aware across the flow.

Floorplanning, placement, clock-tree synthesis, optimization, routing, analysis, and all other steps in the design flow comprehend and optimize across all power domains. This capability enables automatic placement of level shifters, with all power connections completed automatically. The SoC Encounter System also supports the Common Power Format (CPF) to specify advanced power-reduction techniques, from design and verification, through final implementation and signoff.

DESIGN FOR YIELD

Yield presents one of the biggest challenges for advanced process nodes, especially for high-performance designs. The SoC Encounter System optimizes yield issues all the way from RTL to GDSII. At any point in the design flow, designers can perform yield analysis, analyze multiple strategies that can affect and improve yield, and optimize the design immediately in context of all other optimization objectives, including timing, signal integrity, power, and area. The native design-for-yield capabilities of the SoC Encounter System bring visibility and predictability of manufacturing variability to the designer and enable intelligent trade-offs during implementation flow for maximum yield.

MIXED-SIGNAL DESIGN

Today’s high-performance designs have a high percentage of analog components, and the SoC Encounter System handles these mixed-signal designs efficiently without abstracting the information. It also provides interfaces to custom implementation and routing tools and technologies.

CONCURRENT DESIGN OF CHIP AND PACKAGE: FLIP-CHIP SUPPORT

SoC Encounter flip-chip floorplanning and implementation technology enables the concurrent design of chip and package by including package constraints and parasitic effects while designing the IC.

With support for multiple I/O methodologies, concurrent optimization of I/O and core instances, automatic RDL routing including 45-degree support, and accounting for RDL routing during signal/power routing, SoC Encounter flip-chip support eliminates the manual steps in I/O placement and optimization. This mature technology has been proven through multiple customer tapeouts.

PLATFORMS

- Linux (lnx86): 32-bit, 64-bit
- Solaris (sol86, sunv4): 64-bit
- IBM (ibmrs): 64-bit

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more



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