

CADENCE QRC EXTRACTION

Cadence® QRC Extraction, the industry's premier 3D full-chip parasitic extractor that is independent of design style or flow, is a fast and accurate RLCK extraction solution used during design implementation and validation. Its seamless integration with Cadence Encounter® and Virtuoso® design environments ensures ease-of-use and enables rapid analysis to accelerate timing closure.

CADENCE QRC EXTRACTION

As advanced process geometries become more popular, parasitic extraction becomes a necessity not only during the validation phase but also during design implementation. Cadence QRC Extraction is an integrated extraction solution for design implementation and validation at 90nm and below. It includes a full spectrum of technologies for all nanometer-scale design styles including RF, analog, mixed-signal, custom digital, and cell. These advanced capabilities include RLCK extraction, advanced process modeling, multi-corner and statistical extraction, distributed processing, netlist reduction, substrate parasitics extraction, an integrated field solver, an interface to model-based CMP and litho extraction, and more (Figure 1).

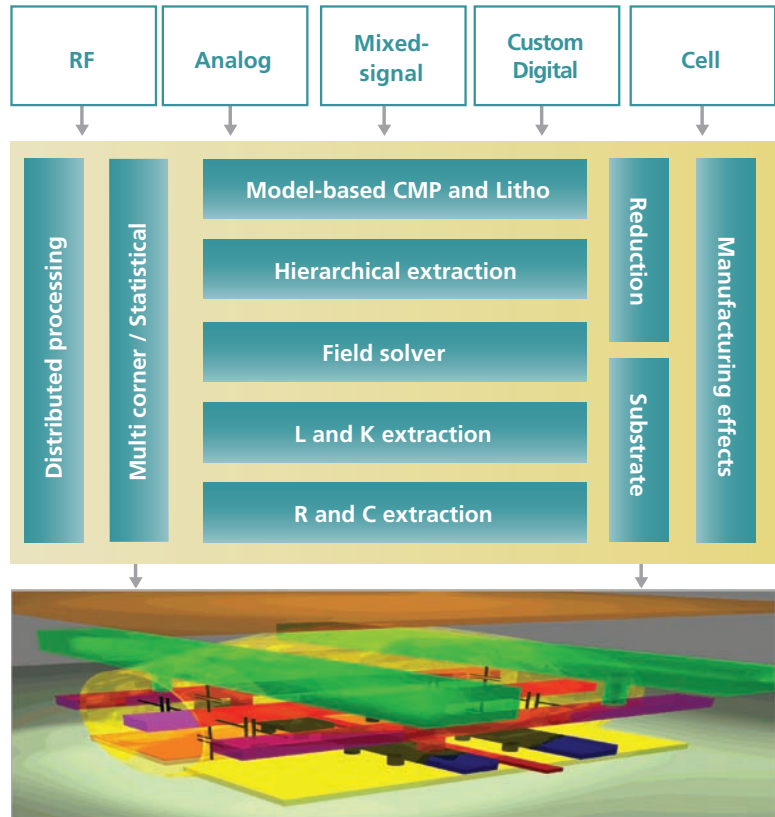


Figure 1: Key components of Cadence QRC Extraction

Cadence QRC Extraction models physical effects found in advanced process technologies to ensure that extracted parasitics match those on silicon. By delivering higher-quality parasitics, it helps designers reduce overall design cycle times and significantly enhance quality of silicon in complex SoC designs. Integrated with Encounter digital design and Virtuoso custom design technologies, Cadence QRC Extraction is the most complete and efficient path to accurate parasitic extraction.

Cadence QRC Extraction is available in L, XL, and GXL configurations. Each of the offerings include both cell-level and transistor-level extraction capabilities.

BENEFITS

- Reduces risk of re-spins with accurate, full-chip extraction including substrate parasitics
- Increases ROI with one-time accurate and consistent setup for ASIC, RF, custom digital, and high-speed analog/mixed-signal designs
- Shortens design cycles by integrating with the comprehensive Encounter and Virtuoso design and analysis environments
- Speeds convergence for timing closure via tight links with analysis technologies (Virtuoso UltraSim Full-Chip Simulator, VoltageStorm® Power Verification, Encounter Timing System)
- Supports advanced process requirements such as optical and CMP effects, process variations, and complex metal/dielectric stack-ups
- Validated silicon models available from leading foundries and IDMs

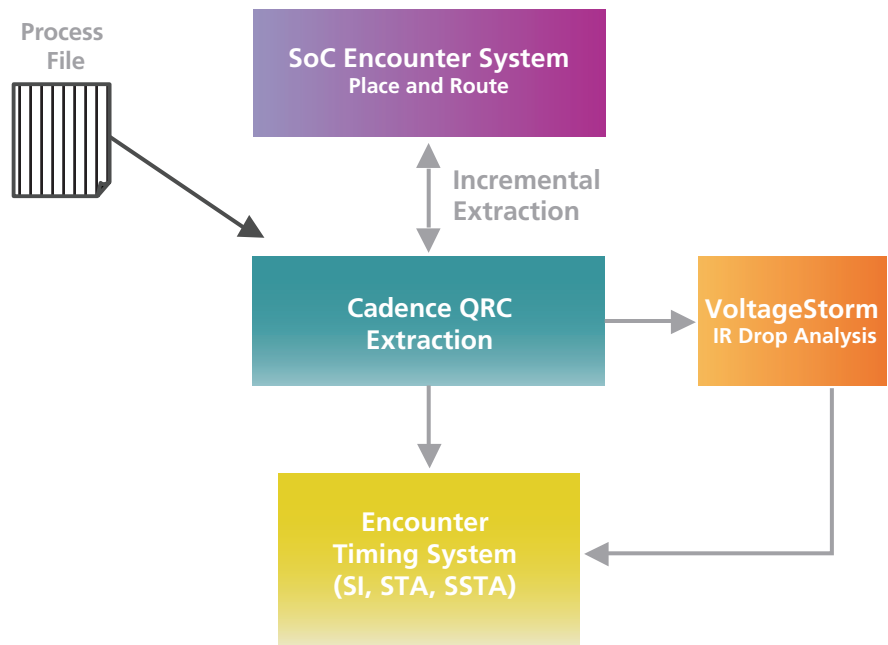


Figure 2: Integration with Encounter place-and-route and analysis technologies

FEATURES

CELL-LEVEL EXTRACTION

QRC Extraction advanced cell-based 3D technology extracts full-chip designs quickly and has the capacity and accuracy for signoff extraction on the largest nanometer designs. Accurate coupling capacitance extraction is a must for crosstalk and power analysis of sub-90nm designs. Integrated with the Encounter design environment, QRC Extraction provides seamless solutions for timing, IR, and EM analysis, signal integrity analysis, and power verification. It can output distributed or lumped, and coupled or decoupled RC data.

Integrated with Encounter technology (Figure 2), QRC Extraction allows designers to reduce design turnaround time dramatically by performing incremental extraction, and to reach timing closure faster by utilizing signoff-accurate extraction data for timing and noise optimization.

TRANSISTOR-LEVEL EXTRACTION

An integral part of the silicon analysis function inside the Virtuoso custom design environment, QRC Extraction supplies the critical parasitic information for optimizing

chip performance and yield. Built on a foundation of patented algorithms and proprietary extraction technologies, QRC Extraction brings the physics of interconnect parasitics into the Virtuoso environment for designing, characterizing, and optimizing chip layouts. Seamless integration with Virtuoso technology enables designers to perform parasitic extraction, backannotation, cross-probing, re-simulation, and analysis within a single design environment for increased productivity.

QRC Extraction provides silicon-accurate resistance (R) and capacitance (C) interconnect parasitic extraction for all process technologies for transistor-level designs including RF, analog, mixed signal, custom, and memory. It provides highly accurate parasitics of both dense and sparse layouts for circuit simulation and analysis. As shown in Figure 3, QRC Extraction integrates with Cadence layout-vs.-schematic verification technologies (Cadence Assura® LVS, Cadence Physical Verification System, Mentor Graphics Calibre) and simulation technologies (Virtuoso Spectre® Circuit Simulator, Virtuoso Spectre RF Simulation Option, Virtuoso UltraSim Full-Chip Simulator).

MULTI-CORNER EXTRACTION

In designs at 130nm and below, a nominal corner extraction and some added margin is no longer sufficient to accurately predict parasitic effects. For example, signal integrity issues can occur at strong, high-temperature conditions. Thus, designers are required to perform extraction at multiple corners, and the number of corners grows as the process geometry shrinks. QRC Extraction can extract multiple corners at once while significantly reducing overall runtime.

STATISTICAL EXTRACTION

QRC Extraction offers statistical capability to efficiently reduce overall extraction runtimes while providing accurate results. It takes into account random variations of parameters like width, thickness, dielectric height, metal resistivity, dielectric constant, via resistance, and temperature. Statistical extraction can significantly reduce extraction runtimes, especially at advanced process nodes.

DISTRIBUTED PROCESSING

QRC Extraction offers a distributed processing capability to efficiently extract multimillion-gate chips. It partitions the extraction task into multiple independent tasks that can be executed in parallel using multiple CPUs and/or machines. Distributed processing can significantly reduce extraction runtimes, especially during the final signoff stages.

ADVANCED SUBSTRATE MODELING CAPABILITY

RF designers need a tool that not only extracts parasitic inductance accurately, but also evaluates the impact of substrate parasitics on their designs. Substrate noise coupling is a growing concern due to higher frequencies, higher integration, smaller feature sizes, and lower supply voltages. Figure 4 shows the effects of including the p-substrate and n-well as part of the substrate model on the extraction result. QRC Extraction includes substrate Rs and Cs for accurate simulation and analysis of RFIC circuits, and allows designers to perform what-if analysis for substrate noise distribution (Figure 5).

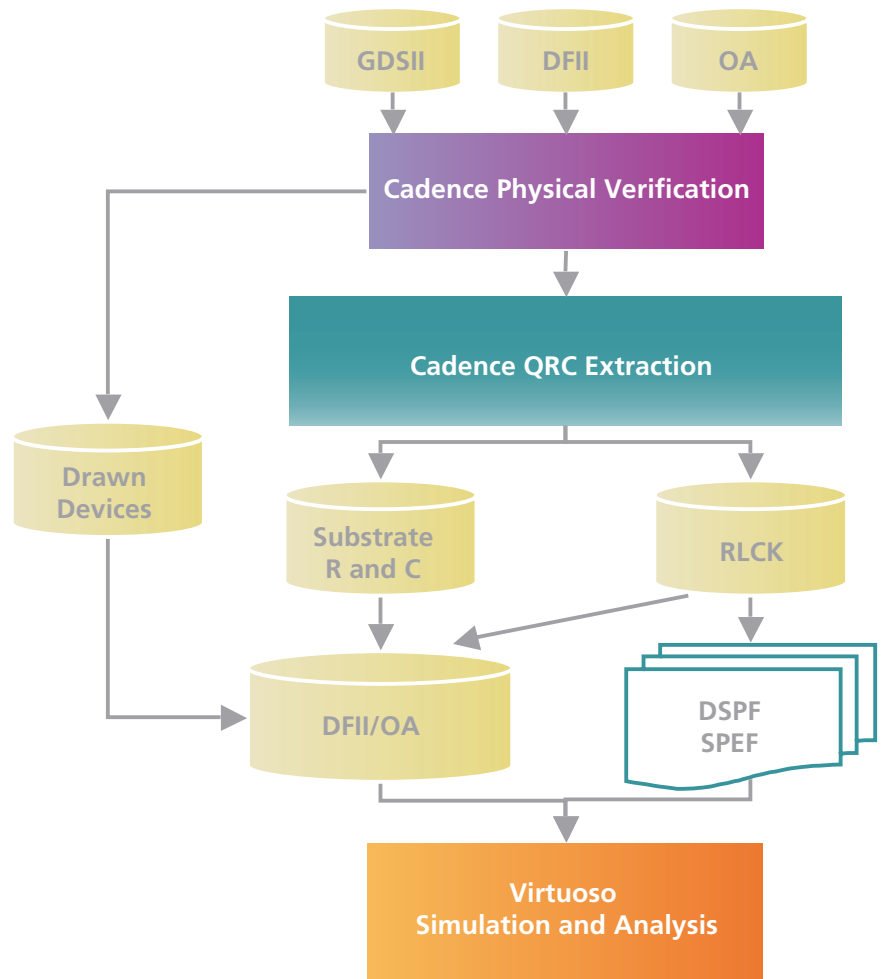


Figure 3: Complete transistor-level RLCK extraction

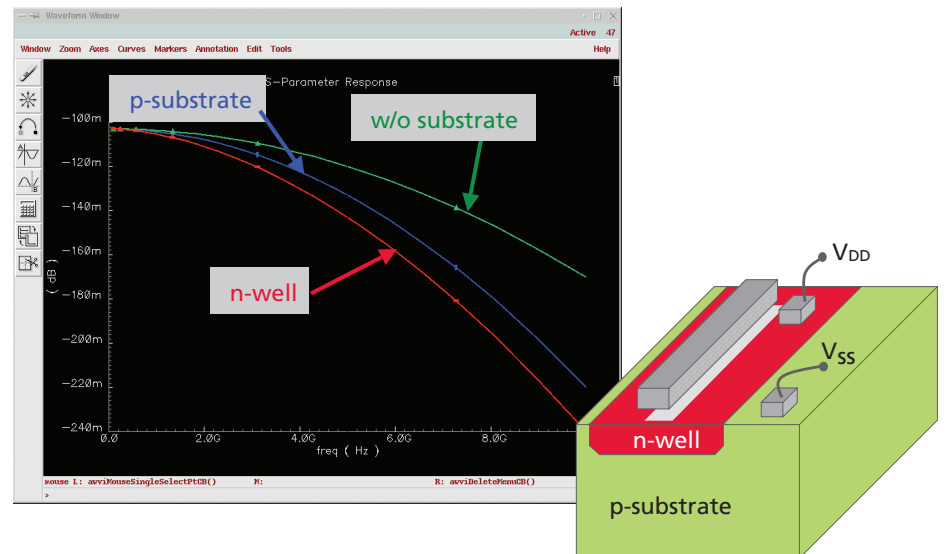


Figure 4: RF interconnect loss

ADVANCED CHEMICAL-MECHANICAL POLISHING (CMP) MODELING SUPPORT

QRC Extraction interfaces to innovative Cadence chemical-mechanical polishing (CMP) technology for modeling full-chip thickness variation and accurately predicting systematic variations in interconnect layer thickness (Figure 6).

QRC Extraction GXL uses the resulting thickness information to generate more precise estimates of parasitic capacitance and resistance and thus more accurate timing analysis and simulation results. By precisely predicting CMP effects with this new capability, designers targeting sub-65nm processes can achieve more accurate timing analysis and simulation, while manufacturing teams can optimize yield.

LITHOGRAPHY-AWARE EXTRACTION SUPPORT

QRC Extraction interfaces to Cadence silicon-correlated electrical DFM analysis technologies. Cadence Litho Electrical Analyzer allows designers to optimize and control the impact of lithography, mask, etch, RET, and OPC effects on chip parameters. Its contour-based analysis technology provides an accurate, model-based solution for designers to minimize the impact of manufacturing variations on design performance (Figure 7). It also uses fab-certified technology to predict contours across the process window and to predict device and interconnect silicon electrical behavior.

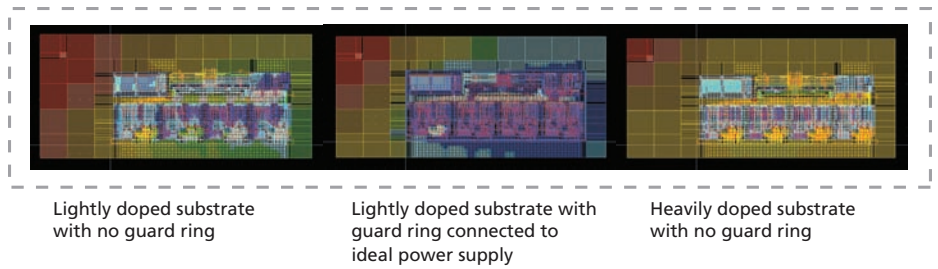


Figure 5: What-if analysis with noise contour map (Cadence QRC Extraction GXL)

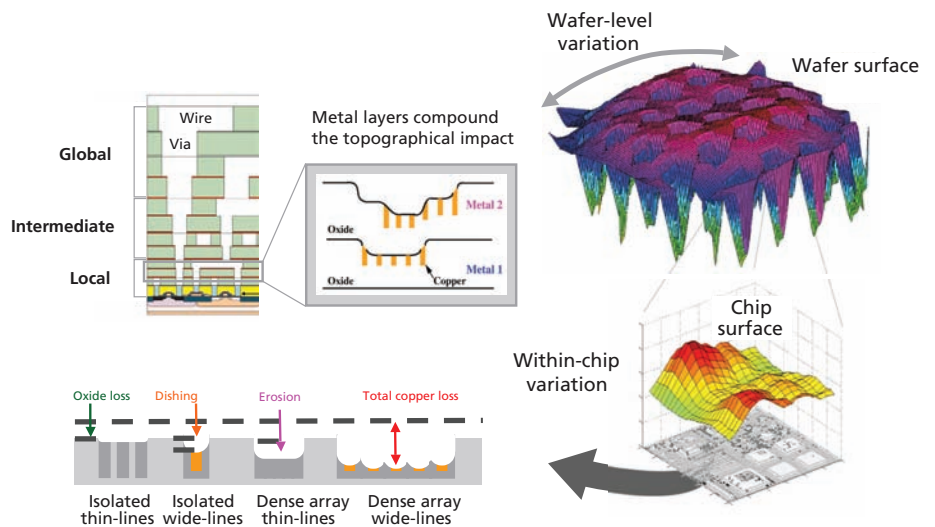


Figure 6: CMP interconnect variation

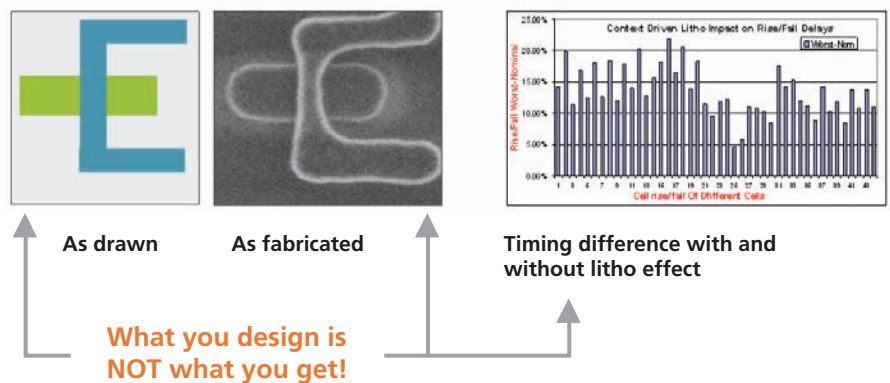


Figure 7: Litho-aware extraction

CONFIGURATIONS

Cadence QRC Extraction is available in L, XL, and GXL configurations for both Encounter and Virtuoso design environments.

SPECIFICATIONS

EXTRACTION MODES

- Black-box, gray-box, or white-box
- Lumped R only, C only, or RC for all nets
- Coupled C for all nets
- Self (L) and mutual (K) inductance extraction
- Fully-distributed RC and RLCK for all nets
- RLCK for selected nets and C for the rest, or vice versa
- Hierarchical transistor-level RC extraction
- Ability to exclude nets, such as power and ground nets
- Critical net and critical path extraction

MANUFACTURING EFFECTS AND ADVANCED PHYSICAL MODELING

- 130nm and below copper, via, and wire-edge enlargement and optical effects
- Conformal, planar, multiple, and low-k dielectrics
- Non-planar processes
- Air gaps
- Trapezoidal conductors

Cadence QRC Extraction Features	L	XL	GXL
Cell-level and transistor-level extraction	x	x	x
Multi-corner extraction in a single run for faster runtimes	x	x	x
Common technology file for consistent results across transistor and gate levels	x	x	x
Supports IR and EM analysis for transistor-level and gate-level designs	x	x	x
Distributed processing support over multiple CPUs	x	x	x
Capacity over 300K (cell) instances		x	x
Hierarchical transistor-level extraction for increased capacity		x	x
Incremental extraction within the SoC Encounter™ System for faster turnaround		x	x
Integrated field solver support for enhanced accuracy		x	x
Support RF analysis with RLCK extraction including substrate extraction		x	x
Advanced support for L and K inductance extraction		x	x
Advanced process support for 65nm and below		x	x
Sensitivity analysis for substrate noise propagation in AMS designs			x
Statistical- or variation-aware extraction support for random process variation			x
Interface to model-based CMP extraction for increased accuracy			x
Interface to litho-aware extraction for enhanced accuracy and reliability			x
Advanced IR/EM support for powerMos designs			x
RLCK reduction to increase simulation speed and capacity			x

- Contact capacitance
- Metal fill
- Local interconnect
- Si, SiGe, and SOI technologies
- Copper technology support (lithography effects, dishing and erosion support)

FOUNDRY SUPPORT

Cadence QRC Extraction process files:

- Certified and supported by leading merchant foundries
- Flow tested and qualified with foundry PDKs
- Development services are available

FORMAT SUPPORT

- Design input formats: GDSII, LEF/DEF, DFII, OA
- Design output formats: Extracted View, DSPF, xDSPF, SPICE, SPEF, xSPEF

PLATFORMS

Sun Solaris (32-bit, 64-bit)

Linux (32-bit, 64-bit)

IBM AIX (32-bit)

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