

# ENCOUNTER LIBRARY CHARACTERIZER

Power and process variation concerns are growing for digital IC designers, who need advanced modeling formats to support their cutting-edge low-power digital design flows. Cadence® Encounter® Library Characterizer provides an automated, high-throughput model abstraction and verification solution. This fast and highly accurate digital characterization technology supports the latest timing, noise, power, and statistical variation modeling formats.

## ENCOUNTER LIBRARY CHARACTERIZER

Major IP providers and digital design teams rely on Encounter Library Characterizer for its simplified setup and accurate model generation for standard cells, I/O cells, and memories. Built on the solid foundation of Cadence SignalStorm® technology—the first characterization solution available for the effective current source model (ECSM)—Encounter Library Characterizer has a long history of providing accurate model generation. IP providers will benefit from its fast and accurate characterization and parallel simulation capabilities, and will be ready to meet current and future customer demand for advanced timing, noise, power, and statistical variation library models.

One challenge designers face when implementing a power savings strategy or moving to a smaller process node is the need for numerous, more advanced sets of standard-cell libraries. For ASIC and CoT designers, this can be a real barrier to realizing their ultimate vision.

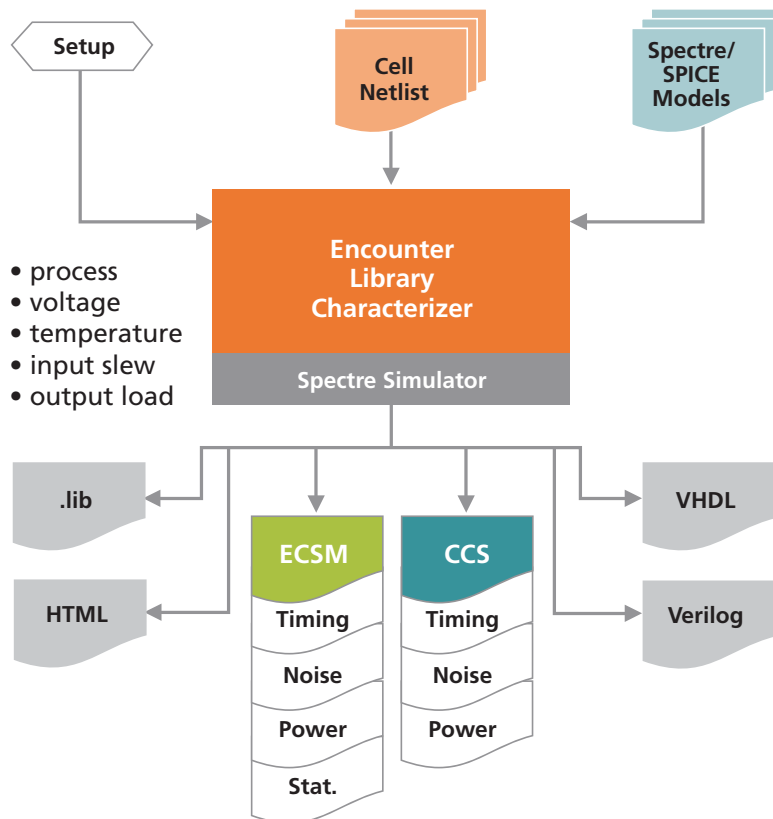


Figure 1: Encounter Library Characterizer delivers a unified system for fast, accurate, and advanced model generation

To implement a particular design strategy and meet their power requirements, designers need custom standard-cell libraries at specialized process, voltage, and temperature (PVT) points. The cost and turnaround time needed to obtain these libraries can limit the aggressiveness of the power-saving strategy employed. Using Encounter Library Characterizer, designers are free to generate any PVT corner in-house, giving them greater flexibility while minimizing the cost of obtaining custom libraries from IP providers (Figure 1).

## BENEFITS

- Unified characterization system delivers faster, simultaneous model generation
  - Automatically creates abstracted models for standard cell and I/O cell characterization and re-characterization
  - Supports IP characterization
  - Now supports memory re-characterization
- Offers high-throughput parallel job execution and management
  - Supports parallel simulation job control
  - Supports simultaneous corners and models
  - Improves performance up to 13x over previous releases
- Supports advanced modeling formats
  - ECSM (effective current source modeling) for delay, noise, power, and statistical
  - CCS (composite current source modeling) for delay, noise, and power
  - Liberty NLDM (non-linear delay modeling)
  - Liberty NLPM (non-linear power modeling)
- Provides automatic and optimized vector generation

- Supports manual vectors
- Enables state-dependent power characterization
- Includes a library validation suite for output library verification, SPICE correlation, and comparison
- Delivers exceptional ease-of-use
  - Supports simultaneous process corners
  - Supports multiple circuit simulators
  - Provides advanced automatic logic recognition for complex gates
  - Offers incremental and detailed runtime status reporting
- Generates HTML data sheets
- Supports adaptive library re-characterization
  - Saves runtime for re-generated libraries for new PVTs, etc.
  - Uses advanced logic recognition when function statement not present

## FEATURES

Encounter Library Characterizer provides a comprehensive characterization solution designed to meet the standard-cell modeling needs of today's advanced digital design flows. It is designed to support advanced low-power, 28nm, multi-corner design methodologies and can characterize for:

- State-dependent pin-to-pin delay
- Input timing constraints (setup/hold/pulse width)
- Power consumption (internal/leakage)
- Input/output pin capacitance
- Input pin threshold voltage
- Output pin transition time
- ECSM and CCS driver/receiver models

## ADVANCED AUTOMATIC LOGIC RECOGNITION

The propagation delay between some input ports and output ports depends on the status of other input ports. Two types of logic are state dependent: complex gates (AOI and OAI) and exclusive logic such as XOR and XNOR. During the logic recognition stage, Encounter Library Characterizer automatically detects state-dependent logic and generates vectors to comprehensively exercise the logic.

## ADAPTIVE LIBRARY RE-CHARACTERIZATION

Designers needing an extra corner, as well as library vendors updating IP libraries, will benefit from the ability to use existing .lib files to save runtime during the characterization process. The library re-characterization feature utilizes information in the timing library—such as function, arcs, I/P slew, and O/P load range—to reduce the dependence on gate recognition by performing automatic sensitization for simulation vectors.

For incomplete cells, adaptive logic recognition technology automatically uses logic recognition to determine the function while preserving the arcs in the original seed library. This enables fast, incremental characterization for different supply voltages and temperatures, process changes, format changes, or underlying subcircuit changes.

## SUPPORT FOR LOW-POWER CELLS

Encounter Library Characterizer supports advanced low-power library model generation and complex state retention power gating (SRPG) cells. For SRPG cells, timing constraints between sleep, save, and restore pins are automatically recognized and generated. It characterizes for:

- Combinational cells with or without a pull-up/pull-down device
- Sequential cells with or without a pull-up/pull-down device
- Sequential cells with balloon structure with or without a pull-up/pull-down device

- Power shutoff cells
- Level shifters

## ACCURATE NLDM CHARACTERIZATION

The industry-standard Liberty (or .lib) format utilizes non-linear delay models (NLDMs) to estimate delay as a function of gate input slew and the network loading on the output. Encounter Library Characterizer accurately generates these models to support synthesis and static timing analysis (STA), and provides a baseline for more advanced modeling formats.

## ECSM DELAY MODEL CHARACTERIZATION

Modeling the voltage impact on delay can be particularly problematic for low-power applications. The effective current source model (ECSM) for timing is an advanced cell driver model that represents the effect of non-linear switching waveforms on cell-based interconnect delay calculation. It has consistently demonstrated superior delay calculation accuracy by modeling a cell's output drive as a current source rather than a voltage source. Current sources are more effective at tracking non-linear transistor switching behavior, and they permit highly accurate modeling of the complex interconnect common in today's largest low-power designs. It is also the only approved standard from the Silicon Integration Initiative's Open Modeling Coalition ([www.si2.org](http://www.si2.org)).

ECSM delay model characterization:

- Used for thousands of tapeouts since 2001
- Delivers accuracy to within 2% of SPICE with non-linear IR drop derating
  - .lib (NLDM) can be off by as much as 20%
- Is an Si2-approved standard
- Offers voltage-based characterization for greater accuracy and ease of adoption

- Supports multi-piece pin-cap modeling for greater accuracy on short, high-fanout nets
- Works with Encounter Digital Implementation System, Encounter Timing System, and third-party tools

## ECSM POWER MODEL CHARACTERIZATION

Encounter Library Characterizer generates ECSM for power inside the .lib format library and enables dynamic or static gate-level power-consumption analysis by characterizing the actual current drawn from the power grid at any given time for individual cells. The extension allows storage of current waveforms at power-grid pins for different combinations of slew and load.

ECSM power model characterization:

- Generates Si2-approved ECSM power extensions
- Characterizes dynamic current signatures of power and ground pins, represented in ECSMs as current waveforms
  - Supports either 2D or 3D lookup tables
  - Generates piecewise linear (PWL) representations of current waveforms
- Can incrementally add ECSM power extensions to existing .lib
- Is supported by Encounter Power System and Encounter Timing System

## ECSM NOISE MODEL CHARACTERIZATION

The risk of signal integrity (SI)-related failures in silicon increases greatly at 90nm and below. Using advanced voltage-in/voltage-out relationships, Encounter Library Characterizer can generate ECSM noise extensions to .lib that enable SI analysis technologies (such as Encounter Timing System) to model the cumulative effects of noise introduced by coupling capacitances in complex scenarios where multi-Vt and multi-voltage devices

co-mingle. The SI extensions are based on the cdB format, which is production-proven in more than 1,000 tapeouts. When used in conjunction with power and timing extensions, ECSM noise extensions will accurately measure the cumulative impact of IR drop and noise on delay and provide a comprehensive view of timing as well as power signoff.

ECSM noise model characterization:

- Generates Si2-approved ECSM noise extensions
- Characterizes for noise delay and glitch models
  - Accurately models the driving stage of each gate noise on delay
  - Models the effective holding resistance of the output stage of the cell for glitch analysis
- Uses advanced voltage-in/voltage-out (ViVo) models that capture the effective cell I-V characteristics
  - Each current model is represented by a ViVo waveform on an input or output pin of a cell
  - 2D lookup table is used to store values of I (Vi, Vo)
- Also considers internal pins
- Is supported by Encounter Timing System and Encounter Digital Implementation System

## CCS TIMING MODEL CHARACTERIZATION

The composite current source (CCS) model is a new, current-based model similar to ECSM that models current vs. time and multi-piece capacitances to enable more accurate static timing analysis. Encounter Library Characterizer provides efficient CCS characterization, which picks current waveform points intelligently to maximize accuracy while minimizing library size.

## CCS NOISE MODEL CHARACTERIZATION

The CCS noise model provides cell-level noise models to enable support for some noise analysis solutions.

Characterization includes:

- Current-based driver model
- Receiver model

## CCS POWER MODEL CHARACTERIZATION

The CCS power model provides additional information for dynamic and static power analysis similar to that provided by ECSM power analysis. Characterization includes:

- DC current
- Output voltage
- Noise propagation
- Miller capacitance

## SILICON-ON-INSULATOR SUPPORT

Partially depleted silicon-on-insulator (Sol) process technology requires special handling during library characterization so that the floating body history effect can be properly modeled during timing analysis. Encounter Library Characterizer can automatically generate the minimum/maximum Sol libraries for each process voltage temperature (PVT) library corner. This enables the history effect to be modeled during static timing analysis when used in conjunction with the simultaneous minimum/maximum mode.

## LIBRARY VALIDATION SUITE

Once libraries are generated for the first time, or when new PVTs are re-characterized from an existing set, it is important to ensure integrity and accuracy. Any problems need to be corrected before they cause hard-to-correct issues in the design flow. Encounter Library Characterizer provides an advanced set of validation tools to help library developers quickly validate the library output and identify problems early.

The `ecsmChecker` utility checks for syntax and semantics issues that would normally be flagged by library parsers. In addition,

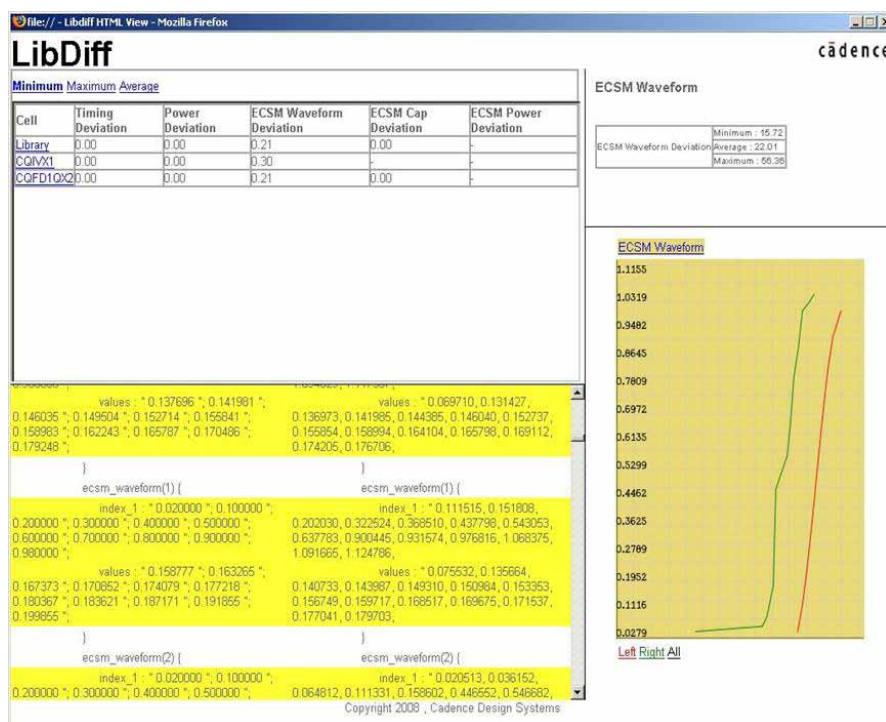


Figure 2: Encounter Library Characterizer offers advanced validation tools

the `ecsmChecker` can perform gross checks on library data to ensure they meet specifications.

The LibDiff utility provides valuable information on the changes from the original seed library. It also checks for syntax and semantic problems with the input libraries (Figure 2). This information is all presented in an easy-to-read graphical interface that shows:

- Minimum, maximum, and average error (absolute or relative) for timing and power, including waveforms
- CCS and ECSM waveforms
- Line-by-line library text comparison

The suite also includes validation utilities which can check the accuracy of the generated libraries compared to static timing analysis and SPICE.

## IP AND MEMORY RE-CHARACTERIZATION

Standard cells are not the only views that need to be re-characterized in order to meet power and accuracy

requirements. Memories and IP blocks are an increasingly large part of today's highly integrated SoC designs and must also be considered when creating new voltage domains or reducing design margins. Often memories and custom macro timing views are only available in a selected set of voltages from a given provider, which may not be optimal for your specific application. Memory generators can also be quite conservative, which can lead to overdesign. Encounter Library Characterizer's ability to generate new voltages and more accurate timing views from existing memory or custom macro netlists improves chip performance and helps you meet your power consumption targets. The memory and IP characterization solution performs fast and accurate re-characterization for:

- Smaller custom macros and memories leveraging Cadence Spectre® Circuit Simulator or Virtuoso® Accelerated Parallel Simulator
- Large memories leveraging Virtuoso UltraSim Full-Chip Simulator (FastSPICE)

Encounter Library Characterizer's memory characterization can generate most standard formats including the advanced current source modeling and power modeling formats.

## ADVANCED SIMULATION AND ANALYSIS

To ensure the flexibility that is critical in today's digital design processes, Encounter Library Characterizer supports the Spectre Circuit Simulator as well as HSpice and Eldo. It also generates statistical timing and leakage power formats used for modeling variation in advanced designs.

## STATISTICAL PROCESS VARIATION MODELING

Process variation—which at 90nm and above had a manageable impact on delay—has a much more dramatic effect as process geometries shrink. For example, a 0.01 $\mu\text{m}$  variation at the 1 $\mu\text{m}$  process node is only 1% of the nominal. However, the same 0.01 $\mu\text{m}$  variation at 65nm is greater than 15% of the nominal.

In traditional static timing analysis (STA), this variability is accounted for by introducing more aggressive gross guardbands and new analysis corners to model different process and environmental variation combinations over multiple analysis runs. The corner-based approach can be overly pessimistic since it can report timing scenarios that have an extremely small likelihood of occurring.

In contrast, statistical static timing analysis (SSTA) signoff uses advanced statistical ECSMs to determine the probability of timing failure over the full range of process variation. SSTA can also account for the variability of the process parameters in a single run. This reduces both pessimism and guardbanding, which in turn decreases area and power

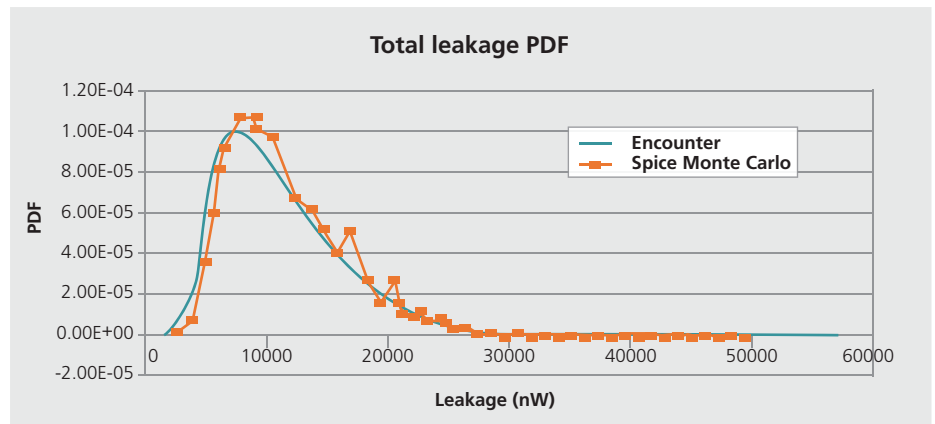


Figure 3: Encounter Library Characterizer GXL uses statistical ECSMs for leakage power characterization to avoid overdesign

consumption, improves chip performance by as much as 20%, and allows designers to explore the potential tradeoff between parametric yield and clock speed.

Advanced features include:

- Si2-approved statistical ECSM generation for greater accuracy
- Sensitivity-based analysis (delay per parameter change)
- Nominal + delay due to changes in parameters
- Within-the-die, die-to-die, and random variation modeling support
- Support for Encounter Timing System, Encounter Digital Implementation System, and third-party tools

## STATISTICAL LEAKAGE POWER MODELING

At smaller process geometries, leakage power begins to dominate the power consumed by CMOS devices. Accurately modeling device leakage is critical to achieving an efficient low-power solution. Existing leakage power analysis techniques use a pessimistic worst-case leakage scenario that has a very small

likelihood of occurring in real silicon. Since cell leakage has an exponential response to process variation—meaning that a small change in process variation causes a major shift in transistor leakage—the probability distribution becomes skewed such that the extreme worst-case scenario has a very small chance of occurring (Figure 3). This leads to aggressive overdesign, overcompensation for IR drop, and potentially unnecessary architectural changes.

The solution is to model the leakage power as a statistical probability to avoid designing to the worst-case limit. This enables designers to target a smaller, more reasonable leakage number, which can be as much as 40% smaller than that from traditional worst-case leakage power analysis. Encounter Library Characterizer GXL is foundry-certified for leakage power characterization using the statistical ECSM format:

- State-dependent exponential leakage power variation with respect to process parameters
- Die-to-die, within-the-die (spatially correlated), and random variation

## PACKAGING

Encounter Library Characterizer is available in XL and GXL base licenses.

## PLATFORMS

- Linux (32-bit, 64-bit)
- Solaris (64-bit)
- AIX (64-bit)
- Sol86 (64-bit)

## STANDARD INTERFACE SUPPORT

- Inputs: SPICE subckt, SPICE models, .lib, setup\_file (for slew, load, operating condition information), and statistical config file (for parameter variation)
- Outputs: .lib + ECSM timing, noise, power, and statistical formats, and CCS
- Simulators: Cadence Spectre, Synopsys HSpice, Mentor Eldo

## CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
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