

Incisive Verification Kit

Easy adoption of advanced, metric-driven verification tools and methodologies

The Cadence[®] Incisive[®] Verification Kit demonstrates functional verification methodologies and technologies by providing workshops, hands-on labs, and tutorial-style documentation plus the ability to integrate and reuse verification IP. Included with Incisive products, the kit is based on the UVM Reference Flow and focused on IP creator and IP integrator verification challenges. Using the kit's real-world design and verification flow, you can improve your skills, discover best practices, and leverage a comprehensive "how to" reference.

Verification Challenges

Functional verification challenges have never been so great. With ASICs now in the multi-million gate range, verification engineers need to generate and manage thousands of tests, deal with frequent changes to the specification and project plan, and coordinate multiple teams and sites. Now more than ever, advanced methodologies are critical to begin the project "with the end in mind"—to set up metrics for verification success that are directly tied to the specifications, and track any changes as closely as possible. When such metrics are captured in an easy-to-read executable form, the verification process itself—along with all the supporting formal analysis, stimulus generation, simulation, and debug activities—can be automated to boost productivity, predictability, and quality. This is the process and promise of metric-driven verification and the Incisive Verification Kit shows you how.

Incisive Verification Kit

The kit offers a comprehensive verification solution tailored to engineers developing IP blocks to complete

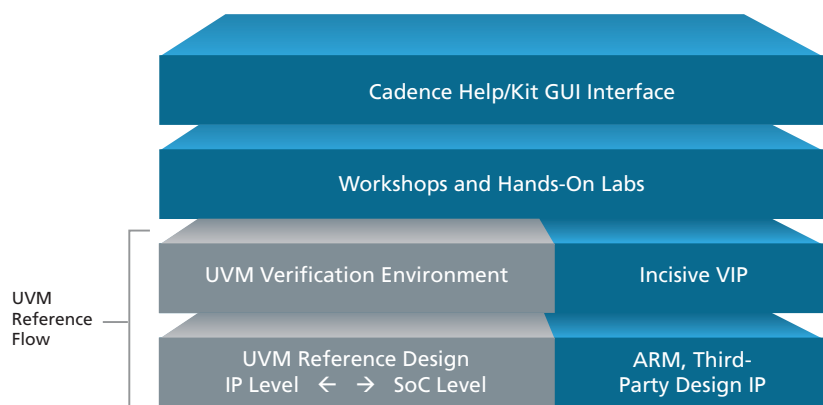


Figure 1: Incisive Verification Kit

SoCs. The environment contains verification methodologies and flows, a realistically challenging Universal Verification Methodology (UVM) reference design, and an advanced metric-driven verification methodology. It also integrates many components from the Cadence portfolio of reusable verification IP (sold separately). The kit can be leveraged to develop your own environment, or can be a learning tool with its interactive design/verification navigator and integrated Cadence "CDNS Help" system.

Powerful Workshops and Labs

Cadence has assembled all of its functional verification workshops and labs and aggregated them into a single kit-based environment. This is a great way to self-teach a specific new technology you would like to learn about, or to determine how to optimize solutions you already have in place. The kit offers the following workshops and labs:

- Metric-Driven Verification
- Low-Power Verification

- UVM Module, Class, and Multi-Language
- Verification Debug
- Introduction to UVM *e* and Specman®
- Assertion-Based Verification
- HW/SW Co-Verification
- Mixed-Signal Verification
- Verification IP Integration and Compliance
- Metric-Driven Acceleration
- TLM Design and Verification

Kit Benefits

- Accelerates and eases adoption of new verification technologies and methodologies
- Increases predictability by automating the verification management and analysis process
- Proves verification productivity by demonstrating how to maximize verification throughput (optimal coverage per cycle)
- Reduces risk and ensures quality through realistic golden verification examples
- Testbench and designs based on standard UVM languages: *e*, SystemVerilog, and SystemC®, as well as Verilog and VHDL
- Shows how-to and best practices with easy-to-follow hands-on labs

Metric-Driven Verification

The Incisive Verification Kit contains the latest methodologies, from low power through assertion techniques, all the way to mixed signal. For design teams moving from directed tests, to advanced verification teams looking to maximize their verification effectiveness, the kit allows you to optimize your learning based on what you know today, and offers an evolutionary approach. It showcases the next methodology beyond coverage-

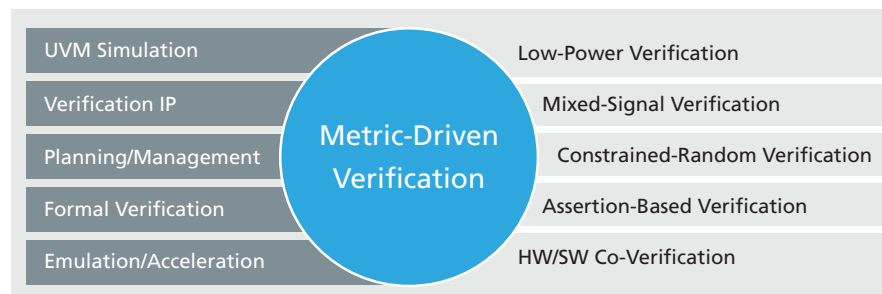


Figure 2: Components of Metric-Driven Verification

driven verification, which is metric-driven verification, enabling users to significantly improve the predictability and productivity of their verification process and, ultimately, the quality of their design. The Incisive Verification Kit demonstrates the methodologies and capabilities in the form of workshops, hands-on labs, and tutorial documentation, with the ability to automatically invoke the needed Incisive tool or verification IP. The kit addresses the verification of both hardware and device software.

Kit Composition and Integration

The Incisive Verification Kit demonstrates multiple verification flows on an OpenCores RISC processor design. The platform consists of both Cadence and third-party IP integrated using AMBA® APB, AHB, AXI, and multi-layer AHB bus fabrics. The kit contains documented best practices and “golden” executable verification plans.

There are two levels of the kit, both of which are supplied with Incisive Enterprise Simulator: the IP-level kit for IP creators and the SoC-level kit for SoC creators. Both the IP and SoC kits use Cadence Verification IP or Universal Verification Components (UVCs). UVCs provide pre-built verification components, from executable plans to protocol compliance management, enabling metric-driven verification out of the box and significantly accelerating your verification productivity.

Reference design highlights

- AMBA-based SoC design using the UVM Reference Flow design
- Integral Cadence and third-party design IP
- Device drivers for all major components
- Low-power domains
- UART design and subsystem for IP-level kit instructions
- MIPI and USB 3.0 design IP provided by Arasan Chip Systems, Inc.

Verification environment highlights

- Integrated CDNS Help environment
- Kit is updated with each major release of the Incisive platform
- Kit license is included with Incisive Enterprise Simulator, Incisive Formal Verifier, and Incisive Enterprise Verifier
- Integrated metric-driven verification techniques utilizing Incisive Enterprise Manager and Cadence VIP portfolio
- Apache Open Source format for many design and verification components
- Low-power and mixed-signal verification techniques demonstrated throughout the kit
- Real-world design/real-world verification environment to maximize learning
- UVCs are provided as both UVM SystemVerilog and Specman/*e*

Installation information

- Ethernet MAC, OpenCores ORIK Processor, UART, and SPI design blocks are open source LGPL licensed
- Embedded software and hardware/software co-verification flows require GNU tools for the OpenCores processor
- The kit is delivered as a tarball operating within a Linux environment
- IP Kit – focused on UART subsystem
- SoC Kit – focused on complete SoC
- The kit documentation system (CDNS Help) can be extracted from the Linux installation and installed on Windows
- The Incisive Verification Kit layers on top of the Open Source UVM Reference Flow, which is updated for each new UVM release

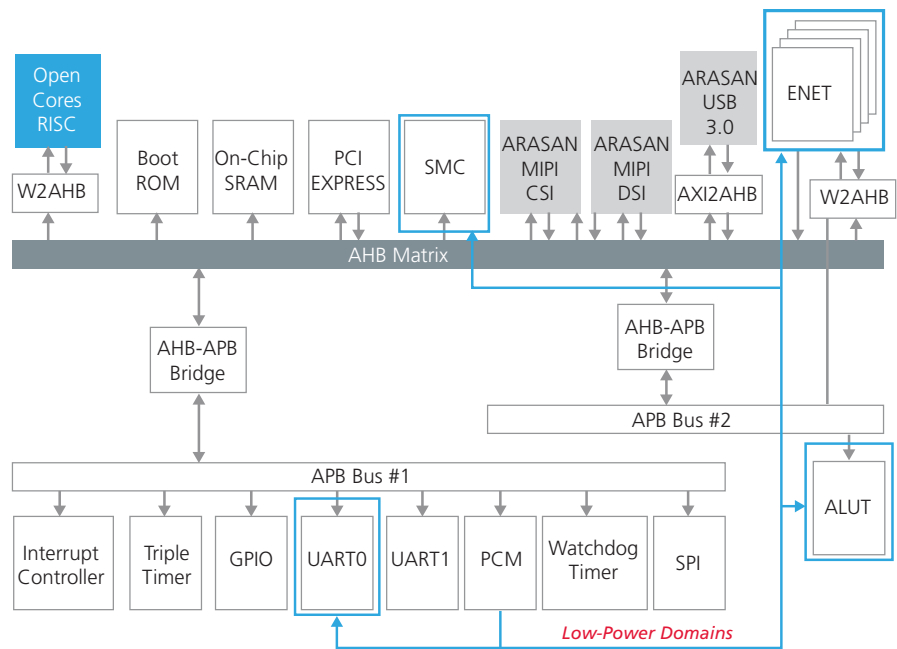


Figure 3: SoC-Level Block Diagram



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com

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