

Encounter Power System

Unified power analysis for faster design optimization and signoff

Even timing-clean designs can fail on silicon due to lowered operating voltages induced by static and dynamic IR drop, increased leakage, and temperature variations. Cadence® Encounter® Power System enables accurate and high-capacity power analysis, helping designers debug and verify that power and IR drop constraints are met across multimillion-gate designs and multiple die—with significant gains in productivity. Integrated with Encounter Digital Implementation System to improve design convergence, it is part of a complete Cadence signoff solution that includes Encounter Timing System and Encounter Library Characterizer.

Encounter Power System

Encounter Power System enables design teams to accurately validate distributed power consumption, IR drop, power rail electromigration, and signal net electromigration (wire self-heat) for complex designs manufactured on all technology nodes. When used with Encounter Digital Implementation System, Encounter Power System enables automated power-rated optimizations driven by analysis results, which improves productivity for design teams.

Encounter Power System is built on production-proven, signoff-quality algorithms and engines that have been used to validate thousands of successful tapeouts. It provides a comprehensive static and dynamic power integrity analysis and signoff solution, combining high performance, capacity, and accuracy with best-in-class debugging capabilities.

Used throughout the design implementation flow, Encounter Power System enables early floor- and power-planning, together with signoff analysis and optimizations for block implementation, chip-level assembly,

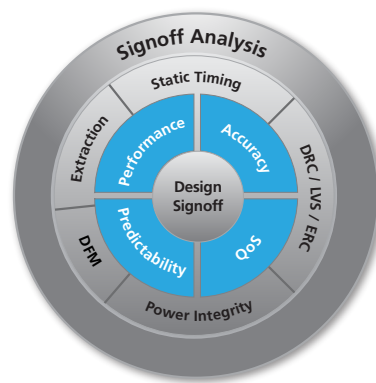


Figure 1: Encounter Power System, combined with Encounter Timing System, offers a complete signoff analysis solution

and pre-tapeout signoff. Using signoff-quality engines throughout the design flow enables consistent, convergent results at every step.

Designed for optimal usability, it has the flexibility to rapidly check that the power rails can supply the amount of power needed during floorplanning, while also enabling accurate, silicon-validated signoff to verify that blocks and the full chip do not suffer from power-related issues.

Encounter Power System drives multiple optimizations to fix power integrity issues, including power rail

and via array sizing, size/location of de-coupling capacitance, size/location of power switches, and I/O placement. It reports all components of power consumption and graphically shows areas of high dynamic power caused by simultaneously switching logic.

Encounter Power System's power calculation engine enables Verilog-based, early gate-level power estimations as well as signoff-accurate distributed power calculation. It leverages Encounter Timing System's signoff timing engine for accurate slew and timing windows needed during vectorless dynamic power calculation.

For power-switch optimization, Encounter Power System can be used to tune the number of power switches while reporting if high rush current could cause local IR drop. The combination of Encounter Timing System and Encounter Power System delivers a comprehensive clock and signal jitter/skew analysis solution. To enable accurate chip/package co-design, Encounter Power System accepts package loading models and outputs a die model of the chip that drives package design and analysis.

Benefits

- Delivers consistent, integrated power and IR drop analysis across the implementation flow, from floorplanning through optimization and signoff
 - Early rail analysis at floor- and power-planning stages allows correct-by-construction power grid design
 - Consistent and accurate power analysis engines (integrated or standalone) improve productivity and convergence
 - Integration with Encounter design implementation platform allows access to physical database and automated engineering change orders (ECOs)
- Provides a unified signoff analysis solution
 - Integration with Encounter Timing System enables analysis of IR drop-induced delay variability across data and clock networks, such as clock jitter and skew analysis
 - Provides consistent engines, interface, and commands across the flow
- Performs comprehensive, hierarchical full-chip and package IR drop analysis
 - Power grid views of analog, mixed-signal, custom-digital, or full digital blocks allow true full-chip IR drop analysis
 - Supports chip/package co-design through package and die model exchange with Cadence Allegro® Package Designer
- Boosts productivity and shaves weeks off tapeout schedules
 - Multi-CPU support ensures high performance
 - Pipelined methodology ensures high capacity and throughput
 - Performs incremental and what-if analysis and exploration
 - Supports the Common Power Format (CPF)
 - Provides a GUI-driven and interactive Tcl command interface
- Allows easy debugging
 - Global power debug speeds up root cause analysis

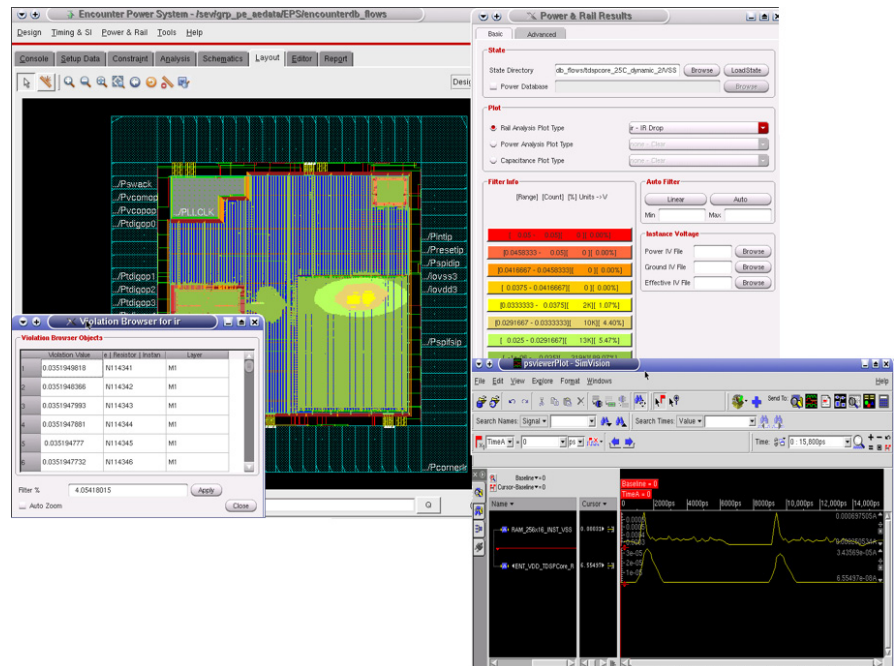


Figure 2: Power and IR drop cross-probing and waveforms

- Integrated waveform and layout viewers enable fast power and IR debugging
- Offers advanced power analysis capabilities
 - Performs analysis across multiple die for stacked-die, 3D-IC/through-silicon via, and system-in-package designs
 - Performs manufacturing-aware extraction for advanced node designs
 - Supports Blech Length for accurate electromigration analysis
- Supported by major foundries, ASIC and IP vendors, and integrated device manufactures

Features

Comprehensive power and power integrity verification

- Flexible, consistent power engine used for power estimation across the implementation flow
- Gate-level power estimation using Verilog input for early power estimation, with full RTL and gate-level VCD and SAIF support

- Accurate post-placement and routing power estimation for power grid optimization and signoff

Easy library generation

- Detailed power grid view (PGV) generation using readily available SPICE subcircuits
- Detailed PGV generation using industry-standard LVS rule decks
- On-the-fly device and coupling capacitance characterization using the embedded Cadence Virtuoso® Spectre® Simulator
- Pass/fail report capabilities to analyze contents of PGVs with guidance on causes of failure
- Layout-aware Power System Viewer (PSViewer) for graphically viewing and debugging PGVs
- Automatic spawning of library generation jobs for macros and memories

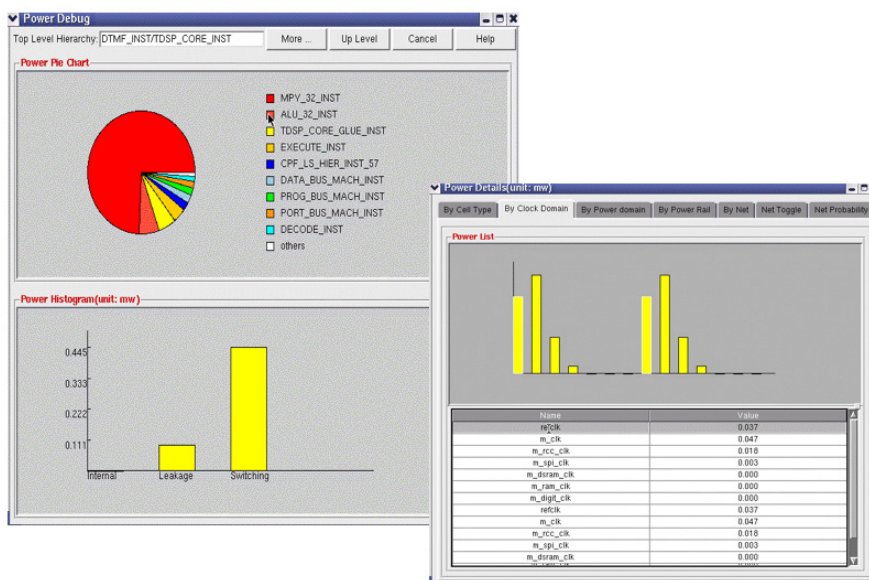


Figure 3: Global power debug

Seamless data import and input-data sanity checking

- Flexible design imports using Encounter database, OpenAccess, or third-party designs
- Embedded design sanity checks such as completeness of LEF library data, timing library data, physical and logical netlist annotation, and SPEF annotation
- Fast structural power grid verification to identify missing vias and disconnected power pins
- Tight integration with the Encounter Timing System signoff timing engine, for seamless transfer of slews and arrival times

Powerful GUI

- Command console with full Tcl support, command completion, history, and context highlighting
- Script editor to evaluate scripts with ability to crosslink and expand Tcl procedures

Easy debugging

- Global power debug for analyzing power consumption at different levels of hierarchy, cell type, power net, power domain, clock domain, etc., with pie charts and histograms
- Integrated full-featured waveform viewer for studying dynamic power and IR drop waveforms, with composite waveform creation capabilities across design hierarchies and clock domains
- Embedded Encounter Layout Viewer with ability to cross-probe power and IR drop information
- Instance-based effective resistance plots with automatic least-resistive path highlighting

- HTML reporting for easy navigation of results
- Fast what-if analysis, enabling quick experimentation

Early rail analysis

Floorplanning and power planning designers can use Encounter Power System engines to rapidly prototype their I/O placement, macro placement, and power grid structure early in the design. Consistency of the engines between early rail analysis and Encounter Power System removes correlation risks, improves productivity, and speeds design closure.

Vector profiling

Encounter Power System includes multiple vector profiling options to help you study VCD profiles textually and graphically. Activity-based vector profiling enables fast identification of high-activity regions of VCDs. A fast vector power-profiling option calculates switching power of the design over time. The accurate vector power-profiling option allows full power estimation of a VCD, with activity propagation capabilities for non-annotated nodes.

Automatic de-coupling capacitance optimization

Encounter Power System can calculate and recommend the amount of additional de-coupling capacitance necessary to limit the dynamic IR drop to user-specified limits. This recommended additional de-coupling capacitance can then drive an automated optimization flow throughout the Encounter platform, where filler cells are swapped with de-coupling capacitance cells. For low-power designs,

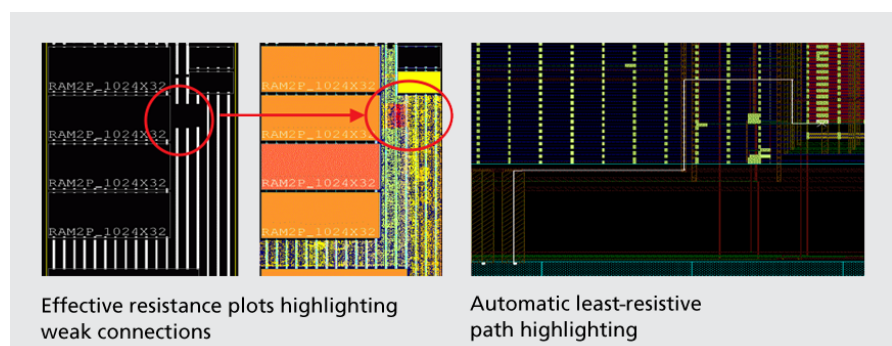


Figure 4: Effective resistance plots with automatic least-resistive path highlighting

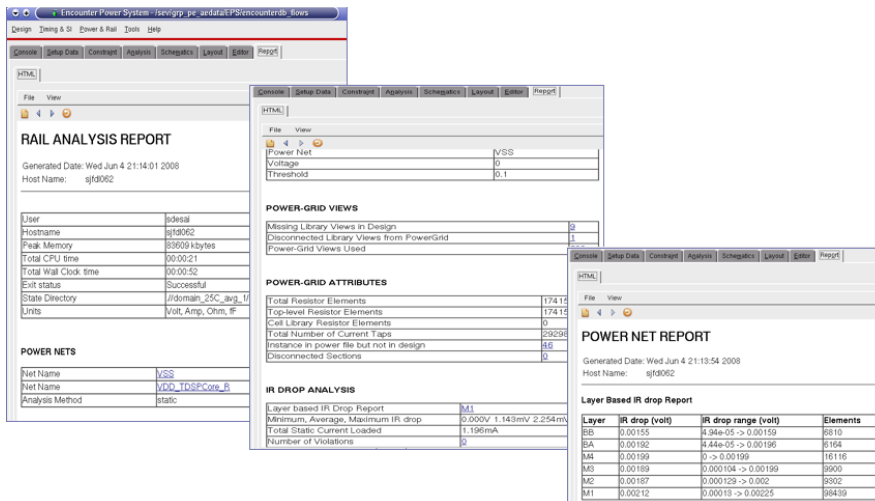


Figure 5: HTML reports

this flow can be used to remove extra de-coupling capacitance cells in the design, improving leakage and yield.

Chip-package co-design

Encounter Power System integration with Allegro Package Designer enables easy hand-off of package and die models. Encounter Power System enables chip designers to create an abstract parasitics and dynamic current profile of the die for package designers. It also takes in two or n-port package models to enable accurate IR drop analysis, taking into account the package effects.

Analysis of IR drop impact on timing and signal integrity

Encounter Power System calculates instance operating voltages based on the switching windows associated with each instance. It then provides this information to Encounter Timing System, which calculates the impact of IR drop on delay and signal integrity-generated noise. Encounter Power System can also generate dynamic IR drop and ground-bounce waveforms for critical paths, allowing Encounter Timing System to accurately trace and analyze such paths.

Clock and signal jitter and skew analysis

The delay variation caused by dynamic operating voltages on the clock networks and signal paths can cause additional set-up and hold violations in a design. By calculating the effective operating voltage of the clock network and signal path elements, Encounter Power System enables Encounter Timing System to more accurately analyze clock jitter, clock skew, and signal delay variability during static timing analysis (STA). This analysis allows Encounter Timing System to identify problematic clock network elements and to create and run a complete jitter-sensitized SPICE trace.

Power-up analysis and power-switch optimization

Many low-power designs now include switched blocks through the use of power switches. These blocks are only turned on when needed, saving leakage power when not in use. Encounter Power System analyzes the power-on and power-off scenarios of these blocks, creating engineering change orders (ECOs) to optimize power-switch size and location. This ensures that the block's rush-current during power-up will not impact the neighboring logic, and that the static and dynamic IR drop within the block is within expected budgets.

Hierarchical IR drop analysis

Encounter Power System uses power grid views (PGVs) as the building blocks for hierarchical power grid analysis. These power models can be created by automated library characterization within Encounter Power System, or following block-level analysis by Virtuoso Power System. After IR drop analysis, both products create PGVs for use in Encounter Power System during full-chip static and dynamic runs. This allows study of IR drop across a complex system on chip that includes digital (ASIC), custom digital, analog, and mixed-signal components and power domains.

Standard Interface Support

- Mandatory design data
 - Timing libraries
 - Verilog
 - SDC
 - LEF
 - DEF
 - SPEF
 - SPICE subcircuits and GDS for design components
 - Power pad location
 - Extraction tech file for QRC or process file
- Optional design data
 - Common Power Format (CPF) file
 - Package model
 - VCD

Platforms

- Sun Solaris 8 or 9 (32-bit, 64-bit)
- HP-UX 11.0 (32-bit, 64-bit)
- Opteron Linux RHEL 3.0 (64-bit)
- Red Hat Linux RHEL 2.1 (32-bit)
- IBM AIX 5.1 (32-bit, 64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

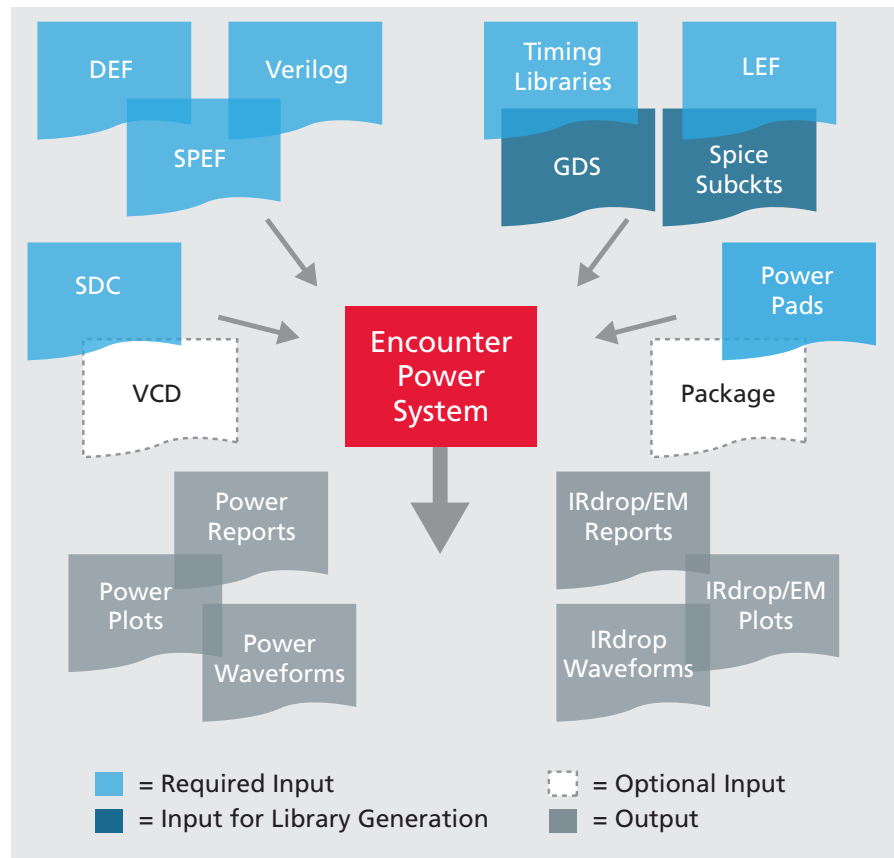


Figure 6: Encounter Power System inputs and outputs