

# VIRTUOSO NEOCIRCUIT

## Circuit Sizing and Optimization

Cadence® Virtuoso® NeoCircuit performs automatic circuit sizing and optimization for custom digital, RF, and mixed-signal circuits. Integrated with the Virtuoso custom design platform, Virtuoso NeoCircuit leverages the Virtuoso Schematic Editor and employs the designer’s simulator of choice to size, bias, and verify circuits interactively with a manual starting point or automatically without any starting point.

### THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

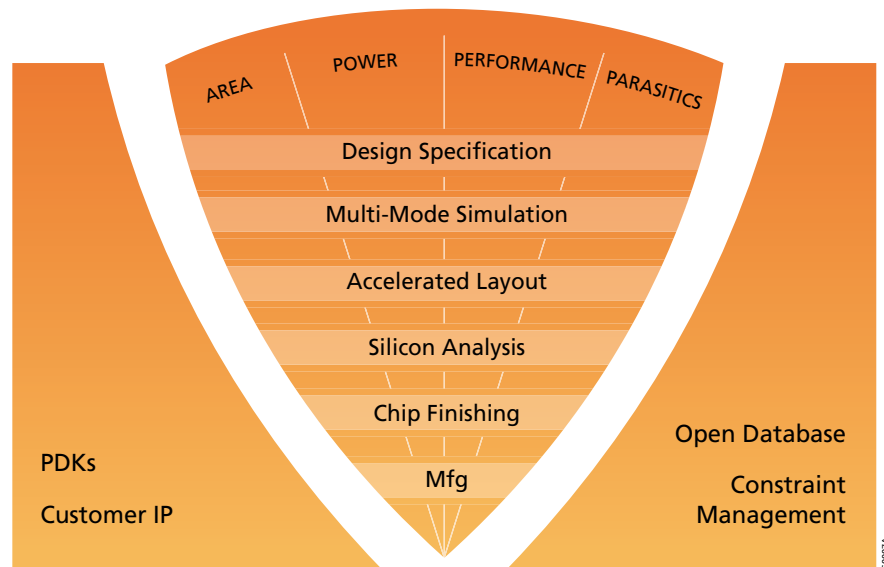


Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

# VIRTUOSO NEOCIRCUIT

Virtuoso NeoCircuit enables designers to automatically size, bias, and verify analog and RF circuits—including LNAs, mixers, opamps, bandgaps, comparators, charge pumps, and VCOs—while using the designer’s simulator of choice. These basic building blocks are used to construct filters, ADCs, PLLs, DACs, etc. Circuit topologies, constraints, testbenches, alternative sized circuits, and layouts are then archived as a library of reusable analog IP.

## BENEFITS

- Increases design productivity up to 10x
- Allows designers to rapidly assess different circuit topologies
- Produces robust designs that work across both environmental and process variations
- Enables IP creation, design reuse, and technology migration

## FEATURES

### DESIGN IP CAPTURE

Using Virtuoso NeoCircuit, designers can capture the design IP in the form of design constraints, archive them on the schematic, check them automatically, and enforce them during sizing.

### INTEGRAL PART OF THE VIRTUOSO CUSTOM DESIGN PLATFORM

Virtuoso NeoCircuit leverages much of the design data that has already been entered in the Virtuoso Analog Design Environment. Testbenches, state files, and calculator expressions are all used during the sizing operation. Virtuoso NeoCircuit also supports hierarchical schematics with hundreds of devices and can handle dozens of performance goals and environmental/process corners. Results of the sizing are backannotated onto the Virtuoso Schematic Editor.

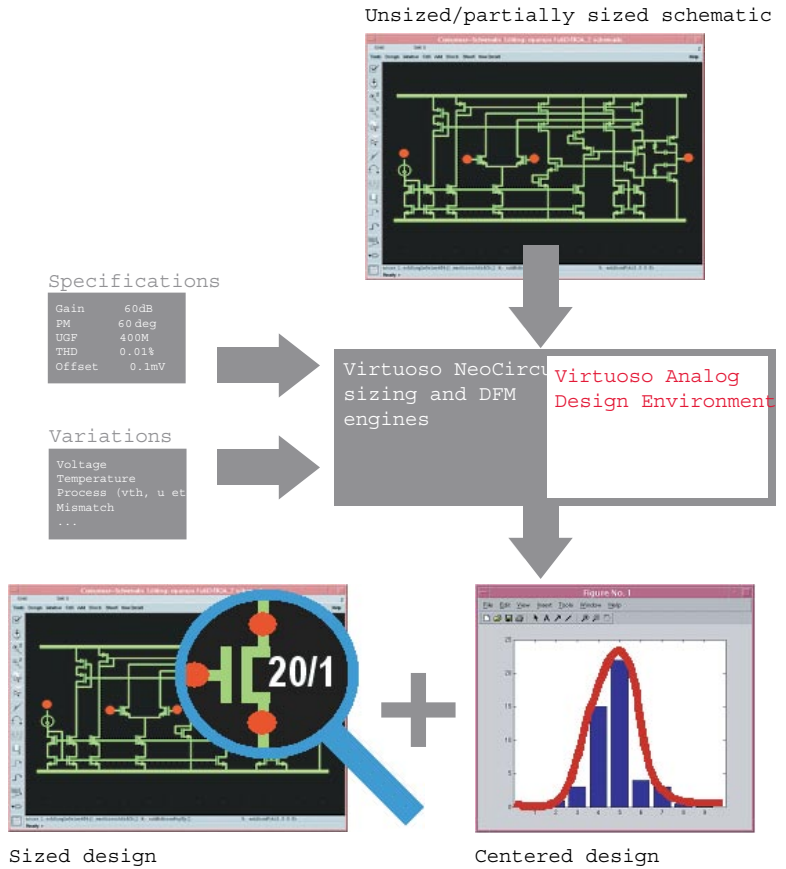


Figure 2: Design centering

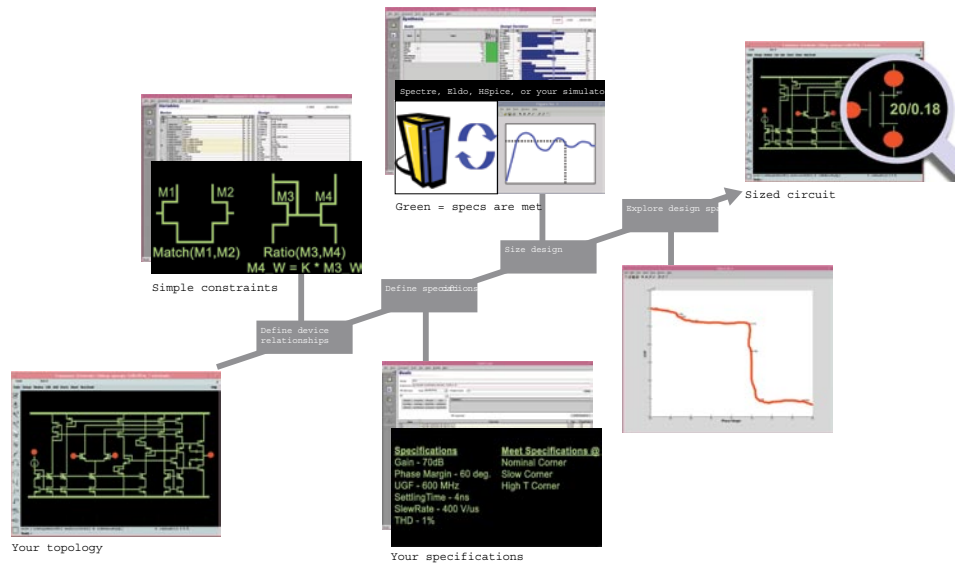


Figure 3: Sizing flow

## IP CREATION, DESIGN REUSE, AND TECHNOLOGY MIGRATION

With Virtuoso NeoCircuit, designers can change constraints to resize them for a technology migration, new performance specification, or engineering change order (ECO).

## UNIQUE SUPPORT FOR DESIGN EXPLORATION

Virtuoso NeoCircuit automatically generates multiple alternative circuit sizing solutions. Users can interact with Virtuoso NeoCircuit to gain insight into their circuit design with feasibility analysis, sensitivity analysis, mismatch analysis, and post optimize “what if” visualization.

## FASTMOS SIMULATOR SUPPORT AND EXTRACTOR SUPPORT

Virtuoso NeoCircuit is integrated with Virtuoso UltraSim Full-Chip Simulator and most third-party FastMOS simulators, enabling large mixed-signal blocks to be sized quickly and efficiently. Virtuoso NeoCircuit is also integrated with most standard extraction tools and can resize devices in the presence of RC parasitics to bring designs back into specification.

## DISTRIBUTED MONTE CARLO ANALYSIS

Virtuoso NeoCircuit enables designers to optimize circuits across variations in the manufacturing process. It supports both global process and local mismatch statistical corners, as well as environmental corners. Using Monte Carlo simulations, Virtuoso NeoCircuit automatically identifies worst-case corners and inserts them into the sizing loop. The design is then optimized over these worst-case corners until the yield of the circuit can no longer be improved. Simulations can be distributed over multiple machines, and a dynamic update of the total yield of the circuit—as well as the yield for each specification at each corner—can be viewed on the designer’s desktop. Designers can also visualize the impact of specific process parameters on circuit performance.

## SPECIFICATIONS

### SYSTEM REQUIREMENTS

- Sun, HP, and Linux hardware with a minimum of 512Mb of memory

### PLATFORM/OS

- Sun Solaris
- HP-UX
- Linux

### DISTRIBUTED PROCESSING

- Parallel analysis capability
- Leverages existing compute farm
- Interface to common load balancing tools such as LSF, Grid Engine
- Graphical monitoring and set up

### INTERFACES

- Dedicated support for Cadence simulators: Virtuoso Spectre® Circuit Simulator, Virtuoso Spectre RF Simulation Option, and Virtuoso UltraSim Full-Chip Simulator
- Third-party simulator for Hspice, ADS, ELDO, and HSim

### THIRD-PARTY SUPPORT

- Support for most FastMOS simulators
- Support for most industry-standard extraction tools

## CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real-world experience
  - More than 25 Internet Learning Series (ILS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, 7 days a week

**For more information**

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