

Cadence Design IP – NAND Flash Memory Controller

A configurable and programmable memory controller

Cadence® Design IP® – NAND Flash Memory Controller is a complete embedded flash controller for synchronous and asynchronous flash interfaces, supporting all ONFi 1 and 2 and Toggle NAND devices. The controller, primarily for use in application-specific integrated circuit (ASIC) and field-programmable-gate-array (FPGA) platforms, offers designers ease of integration, compatibility, performance, and quality.

Benefits Overview

NAND Flash Memory Controller provides compiler options, such as bus width, chip selects, and buffering, allowing for maximum flexibility. The controller supports several power-down options depending on system and chip-level requirements. Optional interface modules include, but are not limited to Advanced High-Performance Bus (AHB), Advanced eXtensible Interface (AXI), and a 3 FIFO interface. Also included are design-specific blocks for error-correction code (ECC) for single-level cell (SLC) and multi-level cell (MLC), command (DMA), and data DMA. NAND Flash Memory Controller supports all standard and advanced commands and provides complete array access, also supporting all major active NAND devices. Check with Cadence for your flash-device requirements.

Features

- Toggle 1 support to 133MTps
- ONFi 1 modes 0, 1, 2, 3, 4, 5
- ONFi 2 mode support 1, 2, 3, 4, 5
- Supports up to ONFi 2.2 and Toggle (66Mhz) operation

- Line-rate hardware detection and correction
- Controller self-configures for flash device type (Id setup)
- Flash data width 8 and/or 16 bits
- Self-configuration and boot support

Key features

- Discovery and initialization
- Logical unit number (LUN) addressing
- Interlaced and non-interlaced addressing
- Source synchronous operation
- Optional command support
- Staggered power-up
- I/O strength support
- Command data and or DMA support

General features

- Option on/off ECC depending on device selection
- Multiple software-selectable ECC solutions

- Optional multi-level bit cell ECC (8, 16, 32, 64, and higher)
- Interrupt generation based on ECC error report
- Standard interface pin labeling
- Data buffering to achieve maximum performance
- Addition of asynchronous FIFOs between the flash controller core and the system interface for speeding matching (AHB, etc.)
- Runs in asynchronous or synchronous modes, dependent on flash device type
- Multiple low-power options
- Supports all NAND command accesses
- Access to spare data area in NAND device
- Simple user interface for on-chip integration
- Support for SLC and MLC boot operation
- Data and command DMA available
- Multi-plane operation
- Read/write cache command support

- Partial page operation
- Small data command support

Asynchronous operation features

- Configurable for bank or chip select options
- Fully programmable timing
- Independent timing for read/write
- Wait state insertion up to three cycles

Toggle and ONFi 2.2

Support for the synchronous ONFi 2 as well as Toggle NAND devices has been incorporated. The controller identifies the device type, issue commands, and supports advanced device features. The physical interface is composed of the link layer and the physical layer (PHY). The link layer supports the interface from the controller to the physical layer so that a standard data bus width can be used. The PHY layer provides timing for control pins, to support synchronous and strobe interfaces and a bypass mode for standard asynchronous operation.

The controller supports ONFi 1 modes 1, 2, 3, 4, and 5 and ONFi 2.1/2 modes 1, 2, 3, 4, and 5 (mode 5, 200MTps, 100MHz). It also offers toggle-mode support for up to 66MHz or 133MTps. The controller supports all ONFi 1 and 2.2 commands, data transfers, and multi-plane operations for two planes. Typical gate count for this controller is less than 100,000 with options for command and data DMA.

Embedded Bus Options

Users can choose from available optional user interfaces. The standard version features a simple user interface designed for on-chip system integration. It has separate address and data buses and command signals. Other standard-interface buses, including Advanced Microcontroller Bus Architecture (AMBA), AHB, AIX, and FIFO, are available. The controller can act as a target or slave device on these buses

Manufacturer	Device Type	Comments
Samsung	SLC/MLC	All known devices
Toshiba	SLC/MLC	All known devices, logical block addressing (LBA) supported
Hynix	SLC/MLC	All known devices
Micron	SLC/MLC	All known devices
ONFi 1	SLC/MLC	All known devices mode 1-5
ONFi 2.2	SLC/MLC	All known devices mode 1-5
Toggle 1	SLC/MLC	All known devices 166MHz

Table 1: Flash device support

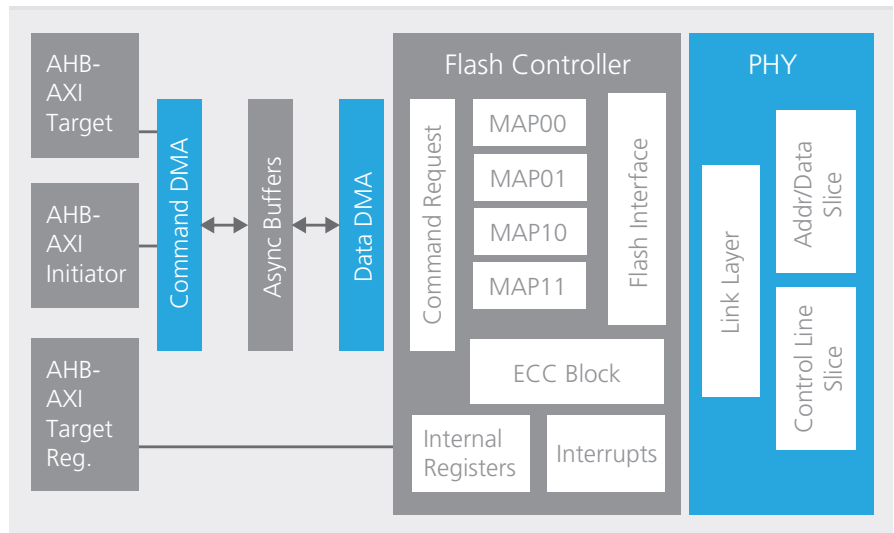


Figure 1: Controller top-level block diagram

ONFi 1 and 2 Modes of Operation

Asynchronous Modes

Parameter	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Unit
	100	50	35	30	25	20	ns

Modes 4 and 5 are EDO-capable.

Source Synchronous Modes

Parameter	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Unit
	50	30	20	15	12	10	ns
	~20	~33	~50	~66	~83	~100	MHz

DMA Overview

Optional DMA blocks are available to optimize performance and reduce software overhead. The additional data DMA permits complete transfers to reduce the number of CPU interrupts. The command DMA works in conjunction with the data DMA to create an intelligent command pipeline to improve the flash array performance. The command DMA requires the data DMA to be included in the delivery—however, the data DMA is self-sustaining. The addition of the DMA IP requires that a master bus interface be used. The DMAs are customized for the user's application.

ECC Overview

With the increase in bandwidth from the synchronous flash devices, NAND Flash Memory Controller supports line detection and correction in hardware, utilizing multi-bit error detection and correction (BCH code). The high performance of the ECC reduces the size of the buffer memory as well as the latency of the controller. Cadence currently supports up to 100 bits of error correction (please check for updates). The controller uses a BCH code to calculate ECC using a 512B or a 1024B ECC sector. Other sizes can be designed for user applications. Currently standard supported page sizes are 512B, 1KB, 2KB, 4KB, 8KB, and 16KB.

The core automatically performs error detection and correction with error logging through internal control registers. It can be configured to generate interrupt on ECC errors.

Physical Layer

The physical layer supports all the compatibility modes as specified in the ONFi and Toggle specification. This includes a bypass mode for ONFi 1 support. The PHY is also available in FPGA and ASIC design flows, and options for a delay-locked loop (DLL) or phase-locked loop (PLL) are available from Cadence. The basic architecture

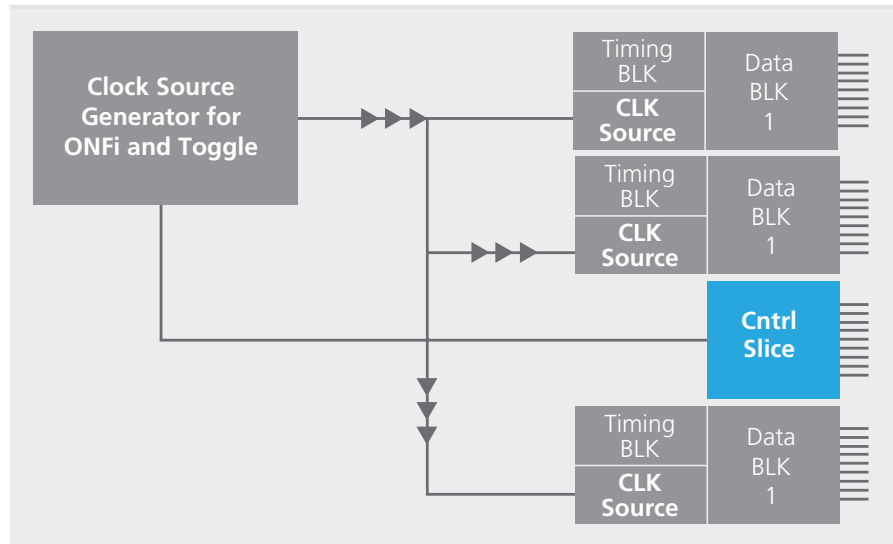


Figure 2: PHY top-level block diagram

uses two physical blocks—one to support the address/data and one for control signals. The physical layer architecture does support single as well as multiple channel designs with a minimum of overhead.

Deliverables

The core is available in ASIC (synthesizable Hardware Description Language) and FPGA (netlist) forms, and includes everything required for successful implementation:

- HDL register-transfer level (RTL) source code (ASICs) or post-synthesis Electronic Design Interchange Format (EDIF) netlist (FPGAs)
- HDL testbench that instantiates the core, bus models of the AHB master and a NAND flash memory device, a clock generator, and processes that compare actual with expected simulation results
- Collection of tests executed directly by the testbench
- Simulation script, vectors, expected results, and comparison utility

- Synthesis script (ASICs) or place-and-route script (FPGAs)
- Comprehensive user documentation, including detailed specifications and a system integration guide

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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