cādence®

Encounter True-Time ATPG

Automatic power- and timing-aware test generation

To reduce cost of test and achieve the highest quality of silicon, engineers need to generate compact, high-coverage, high-quality sets of manufacturing tests. Cadence® Encounter® True-Time ATPG delivers the industry's most comprehensive automated test pattern generation (ATPG) solution. Through a broad array of pre-defined and user-defined static and transition-based faults, multiple on-chip compression architectures, and power-aware test capabilities, Encounter True-Time ATPG achieves the most stringent quality and cost goals.

Encounter True-Time ATPG

Part of the Encounter Test family, Encounter True-Time ATPG offers robust automated test pattern generation (ATPG) engines, proven to generate the highest quality tests for all standard design-for-test (DFT) methods, styles, and flows. It supports not only industry-standard stuck-at and transition fault models, but also raises the bar on fault detection by providing defect-based, user-definable modeling capability with its patented pattern fault technology.

Pattern fault technology is what enables the Encounter "gate-exhaustive" coverage (GEC) methodology, proven to be two-to-four times more efficient at detecting gate intrinsic faults than any other static methodologies available on the market (e.g. SSF, N-Detect).

For delay test, True-Time ATPG includes a dynamic timing engine and uses either circuit timing information or constraints to automatically generate transition-based fault tests and faster-than-at-speed tests for identifying very deep sub-micron design-process feature defects (e.g. certain small delay defects).

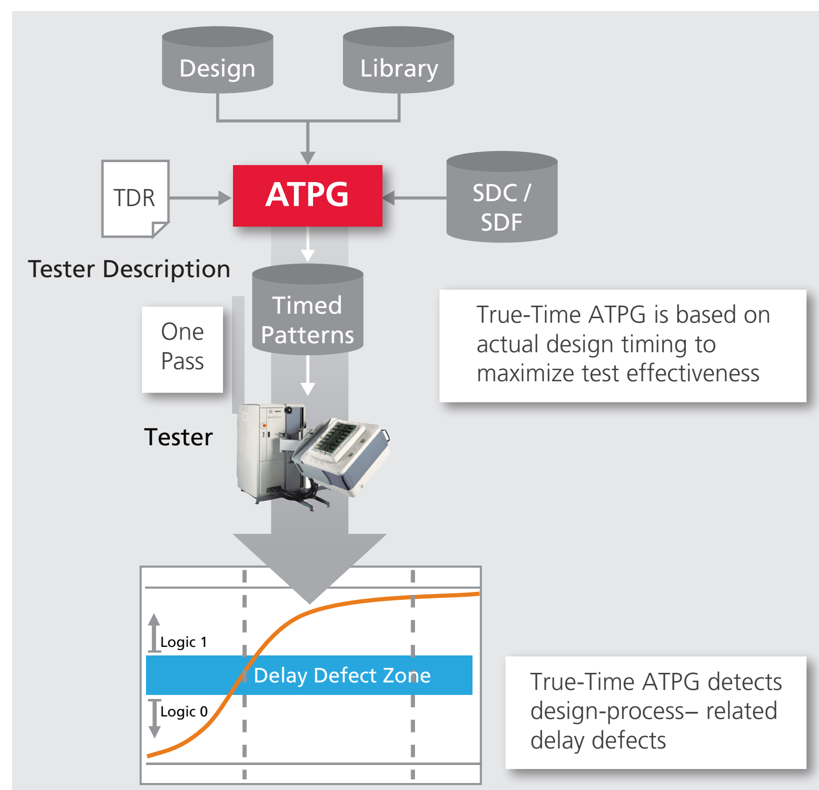

Figure 1: Encounter True-Time ATPG provides a timing-based ATPG engine driven by SDF or SDC information

On-product clock generation (OPCG) produces and applies patterns to effectively capture this class of faults while minimizing false failures. Use of SDF or SDC information ensures the creation of a highly accurate timing-based pattern set.

True-Time ATPG optimizes test coverage through a combination of topological random resistant fault analysis (RRFA) and deterministic fault analysis (DFA) with automated test point insertion—far superior to traditional test coverage algorithms. RRFA is used for early optimization of test coverage, pattern density, and runtime performance. DFA is applied downstream for more detailed circuit-level fault analysis when the highest quality goals must be met.

To reduce scan test time while maintaining the highest test coverage, True-Time technology provides intelligent ATPG with on-chip compression (XOR- or MISR-based). It is also power-aware and uses patented technologies to significantly reduce and manage power consumption during manufacturing test.

True-Time ATPG also offers a customizable environment to suit your project development needs. The GUI provides highly interactive capabilities for coverage analysis and debug; it includes a powerful sequence analyzer that boosts productivity.

Encounter True-Time ATPG is available in two offerings: Basic and Advanced.

Benefits

- Ensures high quality of shipped silicon with production-proven 2-4x reduction in test escapes
- Provides superior partial scan coverage with proprietary pattern fault modeling and sequential ATPG algorithms
- Optimizes test coverage with RRFA and DFA test point insertion methodology
- Boosts productivity by integrating with Encounter RTL Compiler
- Delivers superior runtime throughput with high-performance model build and fault simulation engines as well as distributed ATPG
- Lowers cost of test with pattern compaction and compression techniques that maintain full scan coverage
- Balances tester costs with diagnostics methodologies by offering flexible compression architectures with full X masking capabilities (including OPMISR+ and XOR-based solutions)
- Supports low pin-count testing via JTAG control of MBIST and high-compression ratio technology
- Supports reduced pin-count testing for I/O test
- Interfaces with Encounter Power System for accurate power calculation and pattern IR drop analysis
- Reduces circuit and switching activity during manufacturing test to manage power consumption
- Reduces false failures due to voltage drop
- Provides a GUI with powerful interactive analysis capabilities including a schematic viewer and sequence analyzer

Encounter Test

Part of the Encounter digital design and implementation platform, the Encounter Test product family delivers an advanced silicon verification and yield learning system. Encounter Test comprises three product technologies:

- **Encounter DFT Architect**: ensures ease of use, productivity, and predictability in generating ATPG-ready netlists containing DFT structures, from the most basic to the most complex; available as an add-on option to Encounter RTL Compiler
- **Encounter True-Time ATPG**: ensures the fewest test escapes and the highest quality shipped silicon at the lowest development and production costs
- **Encounter Diagnostics**: delivers the most accurate volume and precision diagnostics capabilities to accelerate yield ramp and optimize device and fault modeling

Encounter Test also offers a flexible API using the PERL language to retrieve design data from its pervasive database. This unique capability allows you to customize

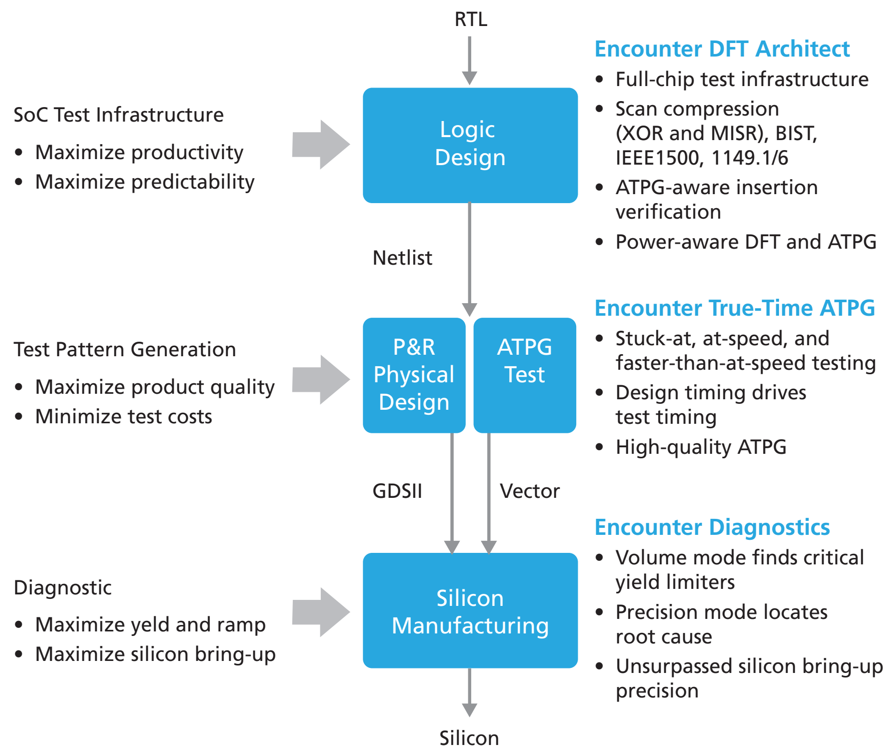

Figure 2: Encounter Test offers a complete RTL-to-silicon verification flow and methodologies that enable the highest quality IC devices at the lowest cost

reporting, trace connections in the design, and obtain information that might be helpful for debugging design issues or diagnostics.

Features

True-Time ATPG Basic

True-Time ATPG Basic contains the stuck-at ATPG engine, which supports:

- High correlation test coverage, ease of use, and productivity through integration with the Encounter RTL Compiler synthesis environment
- Full scan, partial scan, and sequential ATPG for edge-triggered and LSSD designs
- Stuck-at, IDDQ, and I/O parametric fault models
- Core-based testing, test data migration, and test reuse
- Special support for custom designs such as data pipelines, scan control pipelines, and safe-scan
- Test pattern volume optimization using RRFA-based test point insertion
- Test coverage optimization using DFA-based test point insertion
- Pre-defined (default) and user-defined defect-based fault modeling and gate-exhaustive coverage based on pattern fault technology
- Powerful GUI with interactive analysis capabilities

Pattern fault capability enables defect-based testing with a patented technology for accurately modeling the behavior of nanometer defects, such as bridges and opens for ATPG and diagnostics, and for specifying the complete test of a circuit.

The ATPG engine, in turn, uses this definition wherever the circuit is instantiated within a design. By default, pattern faults are used to increase coverage of XOR, LATCH, FLOP, TSD, and MUX primitives. They can also be used to model unique library cells and transition and delay-type defects.

True-Time ATPG Advanced

True-Time ATPG Advanced offers the same capabilities as the Basic configuration, plus delay test ATPG functionality. It uses post-layout timing data from the SDF file to calculate the path delay of all paths in the design, including distribution trees of test clocks and controls. Using this information, you can decide on the best cycle time(s) to test for in a given clock domain.

True-Time ATPG Advanced is capable of generating tests at multiple test frequencies to detect potential early yield failures and certain small delay defects. You can specify your own cycle time or let True-Time ATPG calculate one based on path lengths. It avoids generating tests along paths that exceed tester cycle time and/or mask transitions along paths that exceed tester cycle time. True-Time ATPG generates small delay defect patterns based on longest path analysis to ensure pattern efficiency.

A unique feature of the Advanced offering is its ability to generate faster-than-at-speed tests to detect small delay defects that would otherwise fail during system test or result in early field failures. True-Time ATPG Advanced also uses tester-specific constraint information during test pattern generation. The

Bridge Testing

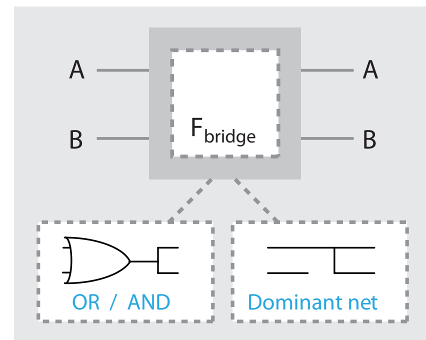

Figure 3: Pattern faults model any type of bridge behavior; net pair lists automatically create bridging fault models; ATPG and diagnostics use the models to detect and isolate bridges

combination of actual post-layout timing and tester constraint information with True-Time ATPG Advanced algorithms ensures that the test patterns will work "first pass" on the tester.

The test coverage optimization methodology is expanded beyond RRFA and DFA-based test point insertion (TPI) technology. The combination of both topological and circuit-level fault analysis with automated TPI provides the most advanced capability for ensuring the highest possible test coverage while controlling the number of inserted test points. DFA-based TPI

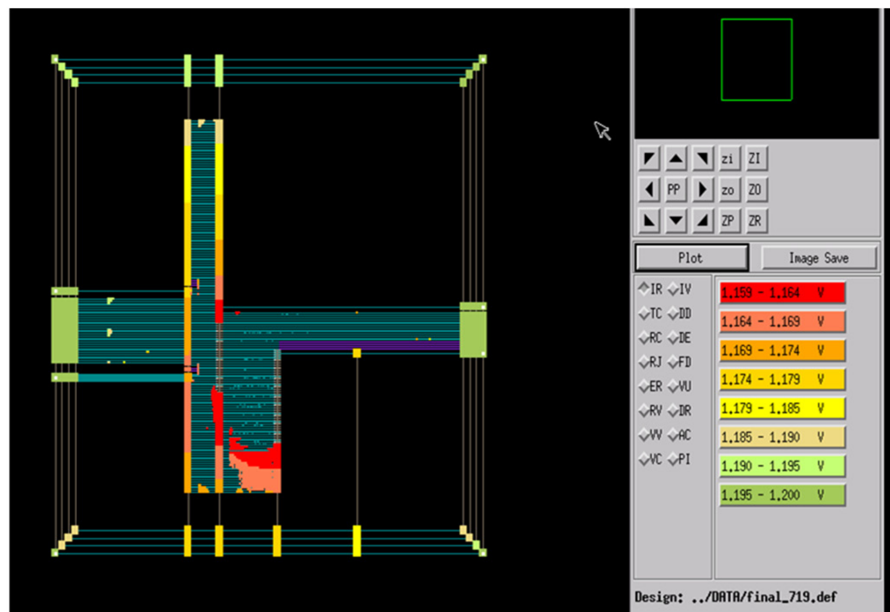

Figure 4: Power-aware ATPG for scan and capture modes prevents voltage-drop–induced failures in test mode

has links to Encounter Conformal® Equivalence Checker to ensure the most efficient, logically equivalent netlist modifications with maximum controllability and observability.

The ATPG engine works with multiple compression architectures to generate tests that cut costs by reducing scan test time and data volume. Actual compression ratios are driven by the compression architecture as well as design characteristics (e.g. available pins, block-level structures). Users can achieve compression ratios exceeding 100x.

Flexible compression options allow you to select a multiple input signature register (MISR) architecture with the highest compression ratio, or an exclusive-or (XOR)–based architecture that enables a highly efficient combinational compression ratio and a one-pass diagnostics methodology. Both architectures support a broadcast type or XOR-based decompressor. On-product MISR plus (OPMISR+) uses a MISR-based output compression, which eliminates the need to check the response at each cycle. XOR-based compression uses an XOR-tree–based output compression to enable a one-pass flow through diagnostics.

Additionally, intelligent ATPG algorithms minimize full-scan correlation issues and reduce power consumption, delivering demonstrated results of >99.5 stuck-at test coverage with >100x test time reduction. Optional X-state masking capability is available on a per-chain/per-cycle basis. Masking is usually required when using delay test because delay ATPG may generate unknown states in the circuit.

Using the Common Power Format (CPF), True-Time ATPG Advanced automatically generates test modes to enable individual power domains to be tested independently or in small groups. This, along with automatic recognition and testing of power-specific structures (level shifters, isolation logic, state retention registers) ensures the highest quality for low-power devices.

Power-aware ATPG uses industry-leading techniques to manage and significantly reduce power consumption due to scan and capture cycles during manufacturing test. The benefit is reduced risk of false failures due to voltage drop and fewer reliability issues due to excessive power consumption. True-Time ATPG Advanced uses algorithms that limit switching during scan testing to further reduce power consumption.

Encounter Test offers a flexible API using the PERL language to retrieve design data from its pervasive database. This unique capability allows users to customize reporting, trace connections in the design, and obtain information that might be helpful for debugging design issues or diagnostics.

Platforms

- Sun Solaris (64-bit)
- HP-UX (64-bit)
- Linux (32-bit, 64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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