

Cadence Design IP: DDR DRAM Controller

Cadence® DDR DRAM solutions are the only fully integrated IP offerings on the market with the features and configurability required to optimize your design and meet your performance, power, and cost targets. With more than 400 design wins ranging from the lowest-power handheld consumer applications to the highest-performance enterprise supercomputers, Cadence Design IP for DDR delivers a solution tailored to your design and is your lowest-risk path to success.

A Complete Solution

The memory subsystem is a core component of any SoC, and the DDR DRAM interface will have a fundamental impact on the performance and cost of your system. Successful designs must support both the latest and legacy devices while delivering the highest performance and the lowest power in all cases.

Cadence Design IP for DDR DRAM supports 10 different DDR SDRAM standards:

- DDR1, DDR2, DDR3, and DDR4
- Low-power DRAM LPDDR1, LPDDR2, and LPDDR3
- Low-voltage DDR2L, DDR3L, and DDR3UL

These memory classes may be freely intermixed to allow popular combinations such as DDR4/DDR3/LPDDR2. A companion Cadence Design IP solution is available for Wide I/O–3D-IC designs using through-silicon vias.

In low-power, wireless, and handheld applications, the Cadence DDR Controller supports the latest mobile LPDDR DRAM standards. Cadence Controllers include advanced low-power and security modules proven to deliver the lowest power possible while maximizing performance in some of the latest smartphone and tablet chipsets.

In enterprise, networking, computing, and other high-performance applications, the Cadence DDR Controller supports the latest high-speed DDR3 and DDR4 devices—either on-board or on DIMM—and it supports the advanced error correction and data protection demanded by these applications.

In consumer and cost-sensitive applications, the performance of Cadence DDR Controller IP maximizes the bandwidth of lower-cost DRAM devices to reduce the overall product bill of materials.

Key Features

- Supports all major memory standards; a Wide I/O Controller is also available
- Supports RDIMM including SSTE32883 and parity
- Supports UDIMM including SoDIMM
- Industry-standard DFI PHY interface
- Priority and quality-of-service features reduce latency
- Flexible paging policy including autoprecharge-per-command
- Two-stage reordering queue optimizes bandwidth and latency
- Coherent bufferable write completion
- ECC allows SECCED over 32 or 64 bits on busses of 16, 32, 64, or 128 bits
- Power-down and self-refresh
- Boot-time programmable DRAM width reduction enables operation on full or half data width while keeping the same memory map
- Supports single- and multi-port host busses (up to 32 busses with a mix of bus types)
- Priority-per-command
- Advanced low-power module can reduce standby power more than 10x and active power by 50%

Silicon-Proven, Scalable Design IP

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, Cadence Design IP has been proven in everything from low-power MP3 players to leading-edge supercomputers. As an active member of the JEDEC standards organization, Cadence can provide IP for emerging standards early in their lifecycles, and can identify and adapt to important changes to existing standards.

Superior Performance

The Cadence DDR Controller is a low-latency design that has been tuned to support the highest speeds of DDR together with legacy devices. With its two-stage reordering algorithms, the DDR Controller is capable of delivering 30% performance improvement over the competition (depending on traffic). Performance-tuning registers driven from memory model files allow optimization of performance according to individual system and memory parameters.

Priority and quality-of-service (QoS) features reduce latency on critical commands by hundreds of clock cycles, and a flexible paging policy (including autoprecharge-per-command) reduces average latency by up to 11 clock cycles. Autoprecharge-per-command allows setting a closed-page policy for transactions with low locality of reference and an open-page policy for transactions with a high locality of reference. This optimizes power and latency for mixed transaction types within an SoC.

Low Power No Matter What the Design

All Cadence Controller configurations support power-down and self-refresh. The optional advanced low-power module includes automatic power-level stepping (based on traffic) and hardware-assisted dynamic voltage and frequency scaling (DVFS). This level of low-power support can reduce standby power by 10x without system intervention, and active power can be reduced by up to 50%.

Application-Targeted Optimizations

Different applications place different requirements on the memory subsystem, so the Cadence DDR Controller includes capabilities to optimize for a wide range of applications. This includes security options such as address range protection, enterprise-class parity and ECC support, and hardware memory BIST.

Unmatched Feature List and Configurability

Differentiating your design means getting the perfect memory controller for your needs. Cadence has developed an unmatched feature list of market-specific differentiating features. Our unique configurability capabilities mean that Cadence can generate a custom DDR controller to your specification—including regressed RTL, documents, and scripts—in as little as 24 hours.

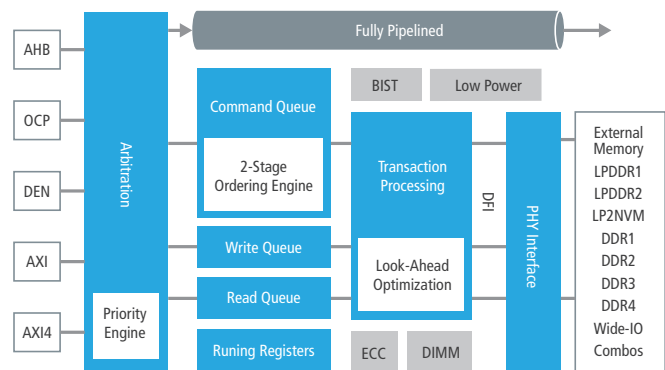


Figure 1: Cadence Design IP for DDR DRAM delivers the lowest-risk path to the highest-performance, lowest-power designs

Supported Interfaces

Host

- Natively supports any mix of ARM® AMBA® 2 (AHB™), AMBA 3 (AXI™), AXI4, and OCP2 interfaces, as well as simple direct access up to 32 busses
- Multi-port solution has choice of bandwidth or QoS-oriented arbitration
- Priority-per-command on AXI3 and OCP, and QoS on AXI4 improves latency and controller QoS, especially for transactions delivered through an interconnect fabric
- Flexible synchronicity allows low-latency synchronous port connection, reduced-latency pseudo-synchronous ratio port connection, or highly flexible asynchronous port connection

Device

- DFI 2.1 and 3.0-compliant PHY interface to connect to Hard and Soft PHY options from Cadence and third parties

Deliverables

- Readable, commented RTL, fully regressed by Cadence for each customer delivery
- 400+ page user manual customized to each customer's exact configuration
- Integration guide
- Synthesis and STA scripts
- Register programming files and script to generate new versions from memory models
- Example testbench with sample tests instantiates memory controller, PHY, I/O, memory model, DFI monitor, and verification IP

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