

Cadence Design IP: DDR DLL PHY

for TSMC40LP, TSMC40G, and TSMC28HPM

Cadence® DDR DRAM solutions are the only fully integrated IP offerings on the market with the features and configurability required to optimize your design and meet your performance, power, and cost targets. With more than 400 design wins ranging from the lowest-power handheld consumer applications to the highest-performance enterprise supercomputers, Cadence Design IP for DDR delivers a solution tailored to your design and is your lowest-risk path to success.

A Complete Solution

The memory subsystem is a core component of any SoC, and the DDR DRAM interface will have a fundamental impact on the performance and cost of your system. Successful designs must support both the latest and legacy devices while delivering the highest performance and the lowest power in all cases.

Cadence DDR DLL PHYs are Hard PHY macros for TSMC40LP, TSMC40G, and TSMC28HPM supporting DDR3, DDR3L, DDR2, and LPDDR2 at speeds up to DDR-1600.

The architecture of the Cadence DLL DDR PHY is a classic slice-based DQS-delay architecture with a 10-year history of reliable design-ins. It has been created for ease of implementation and to be highly compatible with EDA tools from multiple vendors. With a slice-based architecture, the Hard PHY macros offer user flexibility in placement, floorplanning, packaging, and I/O while retaining the reliability and ease of implementation of Hard PHY designs.

The Cadence DLL DDR PHY is an all-digital solution connecting the DDR I/O pads to the DFI interface to the memory controller including alignment of write data, read data capture, and DQS gating. By using an all-digital DLL-based design, both power and area are kept to a minimum, typically under 5mW per data slice.

For consumer, low-power, wireless, handheld and battery-operated devices, the Cadence DDR DLL PHY is a small, power-efficient PHY design supporting the latest mobile DRAM and non-mobile DDR standards.

For other process nodes, Cadence offers range of Design IP for DDR DLL PHY, available as Soft PHY designs for the ultimate in flexibility over process, floorplanning, library, placement, and routing. Cadence Design IP for DDR DLL PHY supports nine different DDR SDRAM standards: DDR1, DDR2, and DDR3; low-power DRAM LPDDR1, LPDDR2, and LPDDR3; and low-voltage DDR2L, DDR3L, and DDR3UL. These memory classes may be freely inter-mixed to allow popular combinations such as DDR3/ LPDDR2.

For enterprise, networking, computing, digital TV, and other high-performance devices, a companion PHASE PHY design is available to reach the highest DDR3 and DDR4 speeds. A companion Cadence Design IP solution is available for Wide I/O–3D-IC designs using through-silicon vias.

Key Features

- Up to 800MHz (DDR-1600) operation, depending on process
- Natively low-latency design
- Read and write data interfaces employing DLL-based delays enable correct data and DQS alignment
- Digital DLL design creates PVT-compensated read and write clocks to the appropriate data paths
- Address and control interfaces for both DDR2/3 and LPDDR2 operation
- 8-bit datapath slice can be repeated to build PHYs of any width
- Individual timing to each data slice supports DDR3 DIMM fly-by timing and unique board topologies

- Register interface for PHY programming, configuration, and testing modes
- Clock gating for low-power operation
- Scan functionality for data slice
- Internal and external datapath loopback mode enables additional functional testing
- Boundary scan muxing built into the core logic facilitates insertion of boundary scan chains between core logic and I/O pads
- I/O pads with termination calibration logic and data retention capability

Silicon-Proven, Scalable Design IP

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, Cadence Design IP has been proven in everything from low-power MP3 players to leading-edge super-computers. As an active member of the JEDEC standards organization, Cadence can provide IP for emerging standards early in their lifecycles, and can identify and adapt to important changes to existing standards.

Low-Power, Low-Area Design

The Cadence DDR DLL PHY is all-digital for the lowest possible power usage and area. Clock gating and DQS gating capabilities serve to reduce power even further.

Superior Ease of Implementation

The Cadence DDR DLL PHY is a third-generation classic DQS-delay architecture created for ease of implementation and to be highly compatible with EDA tools from multiple vendors. The slice-based architecture of the Hard PHY allows more flexibility of placement, floorplanning, and I/O than traditional Hard PHY designs, while retaining the robustness and ease of use of a Hard PHY.

Supported Interfaces

- PC/server DRAM: DDR2, DDR3
- Mobile/low-power DRAM: LPDDR2
- Low-voltage DRAM: DDR3L
- Multi-standard PHYs mixing any of the standards
- Allows your product to penetrate different markets, extends product life, and reduces supply chain risk
- RDIMM including SSTE32882
- UDIMM including SoDIMM
- Industry-standard DFI interface connects to Cadence DDR Controllers or third-party controllers

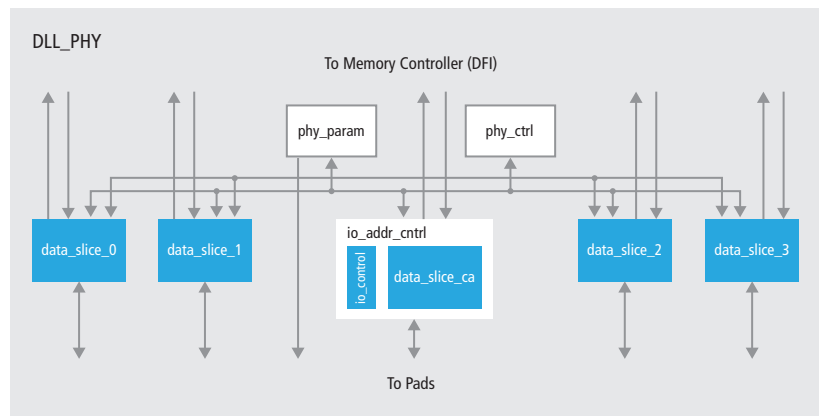


Figure 1: A top-level block diagram illustrates a 32-bit system; other width systems can be implemented by duplication of the data slices

Technology Support

Hard GDSII implementation for TSMC40LP, TSMC40G, or TSMC28HPM (three different Hard PHYs). All PHYs support wirebond or flip-chip implementation.

Deliverables

- RTL Verilog files for all PHY modules including data slice
- Verilog sample testbench with Cadence memory models, encrypted memory controller, and sample tests
- Register configuration files and utilities for programming the sample simulation testbench, controller, and PHY registers
- PHY user guide and implementation guide
- Hardened slice deliverables
 - Liberty timing model
 - Abstract in LEF format
 - Post-layout Verilog netlist
 - GDS layout or P&R db (DEF or Cadence Encounter® format)
 - SDF for backannotated timing verification
 - STA and SI reports
 - LEC report
 - Physical verification reports (DRC, LVS, ANT)
- Synthesis scripts for PHY core level and I/O pad integration
- STA scripts for PHY level, designed to be used at chip level STA or standalone at PHY level, which create SDC inputs to layout and validate timing in the final design



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com