

INCISIVE XTREME SERIES OF ACCELERATORS/EMULATORS

Instant Swap Among Simulation, Acceleration, and Emulation

The Cadence® Incisive® Xtreme® series, part of the Incisive platform's Design Team family, boosts verification productivity with instant swap among simulation, acceleration, and emulation.

The newest products in the series, Incisive Xtreme III Desktop and Incisive Xtreme III System, offer high performance and capacity with desktop density and power, and integrate with evolving simulation-based verification flows. Xtreme III System adds in-circuit emulation capabilities for early system-level verification.



Figure 1: Incisive Xtreme III

INCISIVE XTREME SERIES

The Incisive Xtreme series consists of Xtreme Desktop, Xtreme Server, Xtreme II, Xtreme III Desktop, and Xtreme III System. These products provide a versatile functional verification system for behavioral-, RTL-, and gate-level designs. The latest offerings, Xtreme III Desktop and Xtreme III System, are both fourth-generation server-class hardware verification platforms.

The Xtreme series of accelerators/emulators allows designers to create or modify existing architectures much quicker and earlier in their design flows. Designers can leverage IP from various sources or previous projects and simultaneously simulate, accelerate, and emulate these models. The Xtreme series also enables HW/SW system integration and affirms system performance before silicon is available.

Xtreme products are compact, weigh much less than other products in their class, and use less power, yet they deliver higher performance and capacity. These benefits offer new choices and flexibility, significantly reducing the cost of ownership.

INCISIVE XTREME III

Incisive Xtreme III products extend the capabilities of the earlier generation Xtreme Server by increasing speed and capacity by up to 2x and memory by up to 1.5x, while keeping the same 6U rack-mountable form factor. With its multi-purpose, multi-user, single-database solution for simulation, acceleration, and emulation, Xtreme III products significantly increase your verification productivity and give you complete confidence in your designs. Xtreme III System adds up to 1.4x I/O for in-circuit verification (simulation, acceleration, and emulation) capabilities for early system-level integration and verification.

BENEFITS

XTREME III DESKTOP

- Offers performance in emulation or embedded testbench mode on larger designs from 1,000 up to 100,000x over simulation speeds
- Allows up to 12 simultaneous users
- Delivers typical performance of up to 600KHz on large designs
- Delivers high density up to 72M gates
- Integrates with the common Incisive SimVision simulation debug environment and is script-compatible with Incisive Design Team Simulator
- Instantly swaps among simulation, acceleration, and emulation using a single verification environment/database
- Delivers a one-step compilation process from HDL to runtime
- Expands into multiple applications, such as accelerated SVA and OVL assertions, and SCE-MI 1.1 transaction-based acceleration as well as SystemVerilog DPI support
- Integrates with Incisive Design Team Manager for advanced verification planning and metric-driven closure
- Supports the Incisive Assertion Library (IAL) and Incisive Verification IP (VIP) library
- Emulates behavioral functions with reconfigurable, advanced behavioral processors
- Preserves the native simulation debug environment by supporting all HDL constructs, PLI calls, and verification environments
- Offers simulation acceleration compatibility (with a variety of simulators) for Specman®, Verilog®, SystemC®, C/C++, Incisive Speciman® Elite and VHDL testbenches
- Provides accurate modeling of event-, cycle-, and transaction-based styles

XTREME III SYSTEM

Xtreme III System extends the capabilities of Xtreme III Desktop.

- Provides in-circuit verification (simulation, acceleration, and emulation) capabilities
- Adds up to 6,504 (per fully configured system) user I/Os
- Supports the rich library of SpeedBridge® rate adapters to connect hard targets to the user's design

FEATURES

ONE-STEP COMPILATION AND MAPPING

Design descriptions can be separated into three components: behavioral, RTL, and gates. The Xtreme compiler automatically maps sections that can be emulated with the RCC engine and builds a native-compiled simulation image for sections that remain in the software simulator. A patented hierarchy-extracted mapping technique automatically maps designs onto reconfigurable processors, and the event-driven algorithm of RCC provides optimized usage and high-performance simulation.

SIMPLIFIED LIBRARY AND MEMORY CONVERSION

To maximize density and performance on RCC processors, design library and memory cells are converted into RCC elements. For library cells, the Xtreme library compiler automatically generates the appropriate mapping. For embedded-design memory blocks, a large internal cache and on-board memories are configured to the specific memory type. For complete system verification, large external memories are integrated using an extended memory board or workstation memory.

DEBUG IN SOFTWARE-LIKE ENVIRONMENT WHILE ACCELERATING

The ability of Xtreme accelerators/emulators to swap states between the software simulator and the RCC engine—in real time—makes them unique among hardware verification systems. During simulation, you can swap the state of the RCC engine into the software simulator to interactively debug the design and continue with software simulation. When your circuit is fully debugged and the problem isolated, you can swap the simulation state value back into the RCC engine for maximum performance. Xtreme III System extends these capabilities with in-circuit emulation.

COMPLETE HISTORY WITHOUT RE-SIMULATION

The Xtreme value-change-dump (VCD) on-demand feature gives you access to all node history values from any point in simulation, without re-simulating from time zero. This significantly increases debugging productivity. Waveforms can be generated in either IEEE-standard VCD, fast signal database (FSDB), or SimVision (SST2) format.

ADVANCED BEHAVIORAL EMULATION AND PROCEDURAL CALLBACKS

To address performance bottlenecks as well as overall simulation speed, Cadence has developed several innovative technologies in the Xtreme series of accelerators/emulators. These include an event-based system control, the capability of direct testbench procedural calls from hardware, and behavioral processor technology in hardware. Leveraging this unique hardware architecture, designers or application engineers can map behavioral Verilog constructs or testbench code by hand into equivalent synthesizable RTL code, thus obtaining improved acceleration speed.

Xtreme behavioral processors provide a practical method for emulating non-synthesizable behavioral objects. A unique behavioral emulation capability maintains the performance level of emulation without sacrificing the flexibility of a software simulation environment.

Behavioral constructs are event-driven in nature and require dynamic execution time. Xtreme behavioral processors enable the following for acceleration and emulation:

- Runtime triggering and monitoring
- Automatic and efficient memory mapping (for most types of memory, including complex memory such as CAMS)
- Large arithmetic operations used in datapath-intensive designs
- Behavioral assertion processor technology without gate-count explosion
- Event-driven processing that can sequence operations requiring a dynamic number of steps

IN-CIRCUIT EMULATION WITH XTREME III SYSTEM

Xtreme III System and Xtreme Server can connect directly to a target system and are controlled through a Solaris or Linux workstation for compactness and high-speed communication. The ability to emulate physical hardware with software models simultaneously while also using a software simulation environment for debugging provides the most flexible and accessible system integration solution available.

COMPREHENSIVE SET OF APPLICATION-SPECIFIC SOLUTIONS

Cadence offers a comprehensive set of application-specific solutions to allow rapid adoption of emulation technology. These are pre-validated, in-circuit emulation interfaces known as SpeedBridge adapters, which allow a design under test to be emulated in Xtreme III System in order to interface with a real-world environment.

HW/SW CO-VERIFICATION

The combination of an Incisive Xtreme accelerator/emulator with software models of ARM® processors and a co-verification model of an ARM CPU (with the Xtreme series) provides the most advanced debugging solution for ARM designs and the necessary functionality at each stage of the verification lifecycle. The Xtreme series provides a comprehensive, leading-edge methodology for ARM SoC verification using a unified toolset for HW/SW engineers to verify and debug designs containing ARM microprocessors.

In one package, the Xtreme series provides mixed-HDL logic simulation, simulation acceleration, in-circuit emulation (ICE), HW/SW co-verification using either software models of the ARM CPU or hardware models of the ARM CPU using ICE, and AMBA® bus testbench development.

TRANSACTION-BASED ACCELERATION

Transaction-based acceleration (TBA) is an acceleration mode based on Accellera's Standard Co-Emulation Modeling Interface 1.1 (SCE-MI 1.1) that supports a transaction-level testbench modeling style. TBA utilizes message-level communication between the SystemC testbench components running on the workstation and the rest of the environment running on an Xtreme accelerator/emulator. By communicating at the message level rather than the signal level, TBA reduces the amount of communication, greatly increasing overall acceleration performance (typically from 100–1,000x) over simulation alone.

TBA/SCE-MI-based transactions promote a modeling style that allows users to employ TBA in both accelerated mode and non-accelerated mode, and they provide results that are congruent with simulation. For debug, TBA has the additional advantage of raising the level of abstraction from logic to transaction, such as going from signals to reads/writes.

SCE-MI-BASED INTERFACE

The SCE-MI 1.1-based interface supports testbenches written in C, C++, and SystemC languages to drive the hardware directly. The synthesizable RTL part of the transactor is moved into the hardware engine. The C/C++/SystemC code running on the workstation is interfaced to the accelerator through the SCE-MI-based interface. This can deliver higher performance than an HDL-based testbench.

INCISIVE VERIFICATION IP FOR TRANSACTION-BASED ACCELERATION

Incisive Verification IP (VIP) for transaction-based acceleration (TBA) allows you to run an Incisive simulator either in standalone simulation mode or in TBA mode with total congruency of results. The Xtreme series supports TBA VIP transactors such as PCI Express, Ethernet, AMBA, AHB, and AXI.

ASSERTION-BASED ACCELERATION

Incisive Xtreme products accelerate the Open Verification Library (OVL) and SystemVerilog Assertions (SVA)* through the use of RCC engines and the behavioral processor capability. This advanced verification technique enables design and verification teams to trace faults quickly and accurately to the source, helping them achieve design closure more efficiently. The Xtreme series also supports the Incisive Assertion Library (IAL).

DESIGN TEAM MANAGER INTEGRATION

Xtreme III integrates with Incisive Design Team Manager**, supporting advanced verification planning and metric-driven closure with regression test, failure analysis, and assertion coverage. You can describe and track your tests and assertions in a master verification plan (vPlan), control your regression tests on a high-performance hardware engine, analyze failures, rank tests against coverage targets, and aggregate total system coverage.

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure — virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - More than 80 instructor-led courses
 - certified instructors, real-world experience
 - More than 25 Internet Learning

Series (iLS) online courses

- Cadence customer support that keeps your design team productive
- Cadence applications engineers provide technical assistance
- SourceLink® online support gives you access to software updates, technical documentation, and more — 24 hours a day, 7 days a week

* Please check with Cadence Support for the most up-to-date information on SVA.

** Please check with Cadence Support for the most up-to-date information on Design Team Manager.

SPECIFICATIONS

| FEATURE | DESCRIPTION |
|---|---|
| Architecture | <ul style="list-style-type: none"> • ReConfigurable Computing (RCC) engine, with extended arbiter • Event-based algorithm |
| Supported languages | <ul style="list-style-type: none"> • 1076-1987/1993 IEEE VHDL standard • 1364-1995/2001 IEEE Verilog standard • SystemC 2.1 • TBA extensions, SCE-MI 1.1 • SystemVerilog (assertions and DPI) |
| Software simulator XSIM | <ul style="list-style-type: none"> • Native-compiled with event look-ahead • PLI 1.0/2.0 • IUS compatibility |
| Gate | Up to 72M gates |
| I/O capacities | Up to 6,504 I/Os |
| Runtime performance | Up to 600+ KHz |
| Memory | Up to 18GB of extended memory |
| Programmable trigger generators | <ul style="list-style-type: none"> • Up to 1K probes per trigger • Up to 48 separate trigger generators |
| Debugging | <ul style="list-style-type: none"> • VCD-on-demand (VCD, fsdb, SimVision [SST2]) • Real-time simulation state swap between software and hardware • Assertions • Using behavioral RTL and testbench call-back mechanism |
| Supported operating systems and platforms | <ul style="list-style-type: none"> • Solaris: 8, 9, 10 • Linux: RH 8.0, EL 3.0 • Sun Fire V20z, V40z • Sun V240, V440 • IBM x326 • Sun Ultra 60 • Sun Blade 1000/2000 • Cadence Xhost |
| Verification management and tracking | Integration with Design Team Manager for failure analysis, regression, and assertion coverage |
| Multi-users | Up to 12 |
| Modes of operations | Simulation acceleration, transaction-based acceleration, embedded testbench, assertion-based acceleration, in-circuit verification (simulation, acceleration, emulation) |
| ICE interface | Available only on Xtreme III System |
| <ul style="list-style-type: none"> • Number of Line cards • User I/O per Line card • VCCIO of Line card • Support of input clocks | Up to 12; 1 for each odd board Up to 542 Up to 154 I/Os are software selectable of +3.3v, +2.5v, +1.8v, +1.5v; Other 388 I/Os are +3.3v Yes, with trace buffer |
| Compact size | Height: 10.5 inches (6U) Width: 17 inches; 19 inches with rack-mounting flanges Depth: 22 inches |
| Lightweight | Less than 85 lbs |
| Maximum power | 660 watts |
| RoHS compliant | Yes |

Various configurations are available in the Xtreme series. These are specifications for the Xtreme III product line. Please contact your Cadence Sales Representative for specifications on other products within the Xtreme series.



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