

Cadence Design IP – PCI Express Gen 3 Controller

Industry-leading memory controller IP cores for PCI Express interfaces

Cadence® Design IP® delivers a differentiated, integrated, and proven intellectual property (IP) solution that reduces risk and speeds integration for system-on-chip (SoC) design teams. Silicon-proven Cadence PCI Express Gen 3 Controller IP supports the latest version of the PCI Express® (PCIe) 3.0 base specification released by the PCI Special Interest Group (PCI-SIG) with performance improvements for the PCIe interface. PCI Express Gen 3 Controller was validated using leading PCIe verification tools, including Cadence® Incisive® Verification IP. It's proven in silicon with an external PIPE 3.0 (v0.9)-compliant PCI Express Gen 3 PHY IP and has completed interoperability and compliance testing with commercial motherboards and adapter cards.

Optimized Configuration

Cadence Design IP for PCIe enables chip designers to configure PCI Gen 3 Controller IP for optimal power, performance, and gate-count requirements. Pre-configured PCIe controller cores are also available, providing off-the-shelf IP designed specifically for consumer, enterprise, and mobile applications. PCI Express Gen 3 Controller IP is vendor/process independent and provides configurable support for root complex (RC), endpoint (EP), or dual-mode (switchable RC/EP) devices.

Compliance

As part of the PCI-SIG technical work groups, Cadence actively tracks and enhances its PCI Express Gen 3 Design IP and Verification IP to support the most current release of the PCIe 3.0 base specification. Additionally, the controller has been enhanced with new features to support the latest PIPE 3.0 specification and PCI-SIG engineering change notices (ECNs).

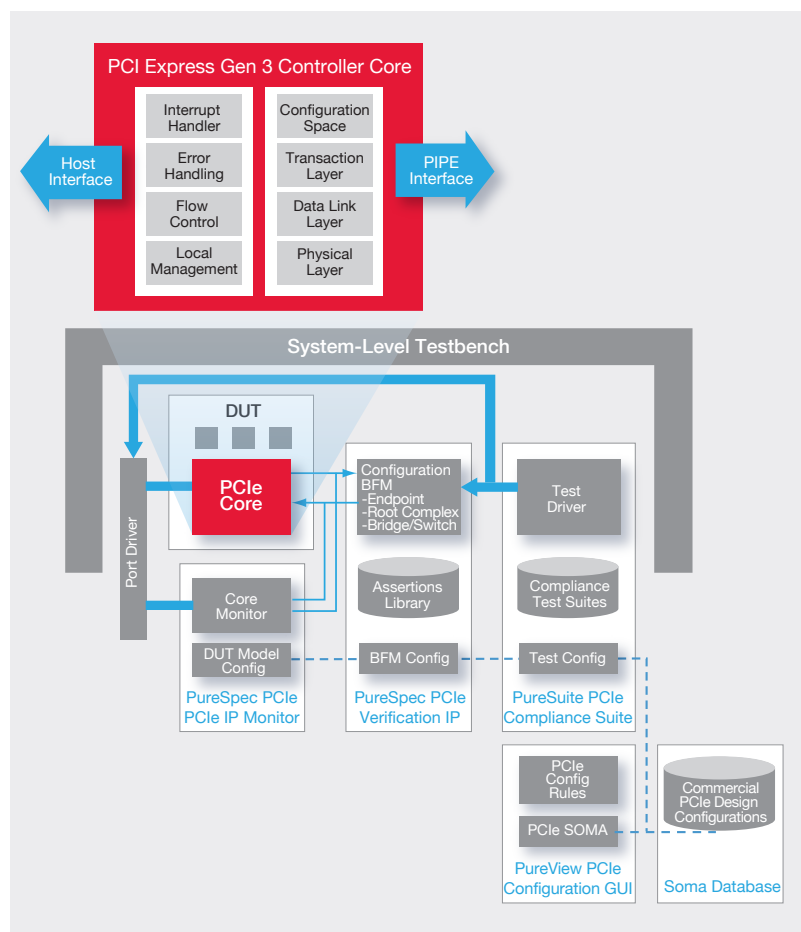


Figure 1: PCI Express Gen 3 Controllers reduce risk, ensure high quality, and speed the deployment of PCIe interfaces in silicon

Interoperability

PCI Express Gen 3 Controller IP is silicon-proven and used in customer production environments, including volume deployment into HP and IBM server-blade products. It has been extensively verified against Catalyst and LeCroy protocol analyzers, and against a wide array of chipsets and adapters from Intel, AMD/ATI, Broadcom, NVIDIA, PLX, and IDT.

Benefits

- Complies with released 3.0 specifications
 - Single Root I/O Virtualization 1.1
 - Intel PIPE 3.0 (v0.9/pre1.0)
 - 32-bit FPGA-variant PIPE interface
- Provides configurable support for RC, EP, dual-mode, and crosslink devices
- Supports the latest ECNs to ensure compliance
 - Internal error reporting
 - ID-based ordering
 - Transaction layer packet (TLP) processing hints (TPHs)
 - Optimized buffer flush/fill (OBFF)
 - Atomic operations
 - Re-sizable base address registers (BARs)
 - Extended tag enable
 - Dynamic power allocation (DPA)
 - Latency tolerance reporting (LTR)
- Includes full power management to reduce power consumption
 - Legacy PCI
 - Active state power management (ASPM)
 - Power management events (PMEs)
 - Beacon
- Includes full interrupt support for INTx, message-signaled interrupts (MSIs), and MSI-X (for PCIe 3.0)
- Delivers high performance, low latency, and high throughput
- Features a highly scalable, pipelined architecture and a small silicon footprint

Features

Gen 3 operation

The controller core supports the latest PCIe 3.0 base specification revision to enable up to 8GT/s lane transfer rates. It automatically negotiates speed and supports link retraining. The controller core is integrated to any Gen 3 PHY via the latest PIPE 3.0 specification and can be operated at 125, 250, or 500MHz with 32-, 64-, 128-, or 256-bit datapaths.

Single root I/O virtualization

The Gen 3 controller core provides full support of the latest address translation service (ATS) specification; Single Root I/O Virtualization (SR-IOV) specification, including physical and virtual function (VF) configuration spaces; VF alternate routing-ID; and functional level reset (FLR) capabilities. This also includes full interrupt, advanced error reporting, and traffic and power management. SR-IOV is an optional capability that can be used with PCIe 2.0 and 3.0 configurations.

Dual-mode operation

Each instance of the core can be configured as an endpoint (EP) or root complex (RC).

Power management

The core supports PCIe link power states L0, L0s, and L1 with only the main power. With auxiliary power, it can support L2 and L3 states.

Interrupt support

The core supports all three options for implementing interrupts in a PCIe device:

- In Legacy mode, the core communicates the assertion and de-assertion of interrupt conditions on the link using assert and de-assert messages

- In MSI mode, the core signals interrupt by sending MSI messages when interrupt conditions occur; it supports up to 32 interrupt vectors per function, with per-vector masking
- In MSI-X mode, the core supports up to 2,048 distinct interrupt vectors per function with per-vector masking

Credit management

The core performs all the link-layer credit-management functions defined in the PCIe specifications, and all credit parameters are configurable.

Configurable flow-control updates

The core allows flow-control updates from its receive side to be scheduled in a flexible manner, enabling the user to make tradeoffs between credit-update frequency and its bandwidth overhead. Configurable registers control the scheduling of flow-control updates to the data link layer packets (DLLPs).

Replay buffer

The core incorporates fully configurable link-layer replay buffers for each link. Designed for low latency and area, it can maintain replay state for a configurable number of outstanding packets.

Host interface

The datapath on the host interface is configurable to be 32, 64, 128, or 256 bits. It may be an advanced extensible interface (AXI) or host application layer (HAL) interface.

HAL interface

Five distinct, simple interfaces for master, memory, I/O, messaging, and interrupt transactions hide PCIe complexity:

- The memory read/write interface is for access to memory controllers or direct memory access (DMA)
- The master read/write interface is to initiate requests from the endpoint as a bus master
- The I/O interface supports PCIe I/O transactions
- The messaging interface supports customer messaging across PCIe
- The interrupt interface supports all interrupts from the user application to the Cadence PCIe core

Multiple PCI functions

The core includes configuration space registers for up to eight separate PCI functions, or up to 256 functions with alternate routing-ID, which are active when the core is configured as an EP.

Local management interface

The core provides a 32-bit management interface through which firmware can read and write registers in the core. Software can access registers in the configuration space as well as local management registers (which contain the configuration settings of the core, debug registers, status registers, etc.)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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