

# Incisive Verification IP for the ARM AMBA Protocol Family

Cadence<sup>®</sup> Incisive<sup>®</sup> Verification IP (VIP) for ARM<sup>®</sup> AMBA<sup>®</sup> protocols provides metric-driven verification of protocol compliance, enabling comprehensive testing of interface IP blocks and SoC designs. Customers have verified more than 1,600 AMBA protocol-based designs using Cadence VIP, which complies with industry-standard verification methodologies and languages. The included Compliance Management System analyzes coverage results against the verification plan and eliminates the guesswork from knowing when to tape out. AMBA is one of 30+ protocols supported by the Cadence VIP portfolio.

## Key Features

### Stimulus

- Hundreds of generation constraints enable targeting of coverage holes

### Checks

- 290+ automated protocol checks
- Full access to transactions for custom scoreboards
- Conveniently add DUT-specific checks

### Coverage

- Coverage model with thousands of pre-defined buckets

### Compliance Management System

- Automates stimulus generation and checking of protocol compliance
- Integrates with Incisive metric-driven verification technologies

## Capabilities

- Verifies AMBA AHB<sup>™</sup>, APB<sup>™</sup>, AXI<sup>™</sup>, and AXI4<sup>™</sup>
- Supports AHB, AHB-Lite<sup>™</sup>, Multi-Layer AHB, APB, AXI, AXI4, AXI4-Lite<sup>™</sup>, and AXI4-Stream<sup>™</sup> interfaces

- Generates and drives constrained-random bus traffic as a bus master
- Responds to bus traffic as a bus slave
- Monitors, checks, and collects coverage on bus traffic and interconnect
- Includes hundreds of assertions for formal compliance verification
- Integrates with SystemVerilog and e language testbenches
- Complies with the Universal Verification Methodology

- Includes a Compliance Management System for automated protocol verification

## AXI4 UVC

The AXI4 UVC provides support for the AXI4, AXI4-Lite, and AXI4-Stream protocols. Throughout 2010, this UVC is available to customers on a limited basis as the AXI4 specification continues to evolve.

## AXI Master Verification

The AXI UVC verifies the design under test (DUT) by providing active slave agents for generating stimuli and passive master agents for

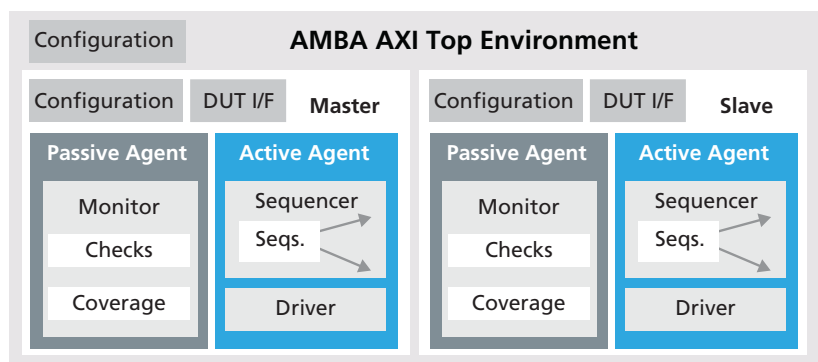


Figure 1: AMBA AXI UVC architecture

“The strength of AMBA has always been centered around its broad industry adoption and EDA support. As a leading EDA company, Cadence has enabled the embedded community with AMBA-based design and verification tools for years, and we look forward to their continued strong support for our newest AMBA 4 on-chip interconnect specification.”

- Keith Clark, VP and GM, Fabric IP Processor Division, ARM

checking the protocol and collecting coverage. Slave response attributes may be configured according to multiple parameters including:

- Write burst response
- Write response delay
- Address ready delay
- Out of order transaction completion
- Read data control
- Emulate memory

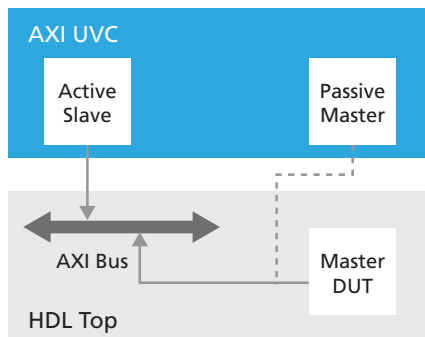


Figure 2: AXI UVC functioning as master

### AXI Slave Verification

The AXI UVC verifies the DUT by providing active master agents for generating stimuli and passive slave agents for checking the protocol and collecting coverage. Master burst attributes include:

- Fixed, incrementing, and wrapping bursts
- Normal, exclusive, and locked access
- Single byte to 128-byte transfers
- 1 to 16 transfers per burst
- Programmable transmit delay
- Out of order transaction completion
- Error injection: malformed burst, transactions to unmapped addresses
- Address valid delay

- Verify-memory consistency
- Write data control
- Driving write transfers before the address phase

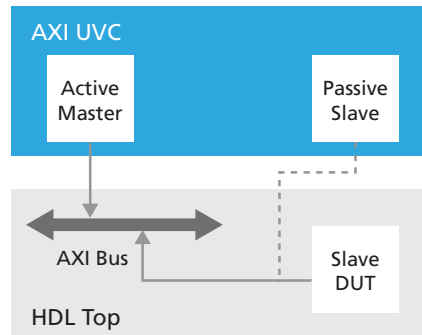


Figure 3: AXI UVC functioning as slave

### AXI Interconnect Verification

The AXI UVC provides a passive interconnect agent for checking the protocol and collecting coverage. On each port it provides active or passive AXI slave or AXI master agents. The interconnect agent supports:

- Monitoring of data
- Any number of input/output ports
- Input/output ports connected to another interconnect
- Each port having a different clock, ID width, endianness, number of concurrent read/write bursts
- Defining delays for read/write addresses or data channels or for the entire interconnect
- Unmapped bursts not passed to output ports

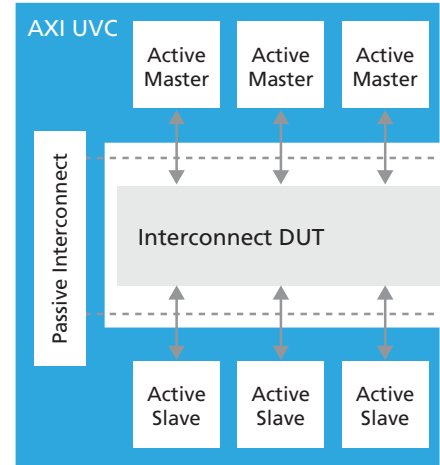


Figure 4: AXI UVC verifying interconnect

### Formal Verification

Formal analysis uses properties to define the desired behavior of a design within the design’s environment. There are two types of properties:

- Assertions: Properties that express the desired behavior of a design under verification
- Constraints: Properties that express the behavior of the environment

Formal analysis exhaustively verifies that the assertions hold true for all possible stimuli that fit within the constraints. This contrasts with simulation, which verifies that a design behaves correctly only in response to a given set of stimuli. However, both technologies can also be combined to leverage their respective strengths.

Incisive VIP for the AMBA protocol family includes hundreds of properties to formally verify compliance with AXI, AHB, and APB specifications. The properties are fully validated, so you can plug them right into your design without fearing that false-negative results will derail your debugging effort.

Since no stimulus or testbench is required, designers can get a jumpstart on the verification process before handing off the design to the verification team.

Cadence supports both “pure” formal analysis with Incisive Formal Verifier, and integrated formal and dynamic simulation technologies in Incisive Enterprise Verifier

### Focus On Verification

Incisive verification IP is independently created and tested against external design IP sources to provide fully objective validation. This approach prevents the bug transfer that can occur when design IP and verification IP are co-developed.

XL. Both tools leverage the familiar SimVision GUI, allowing quick bring-up and efficient use of AMBA VIP.

### Single AHB Module Verification

A single AHB module can be one of the following AHB agents: master, slave, arbiter, or decoder. The AHB UVC verifies the module agent by providing AHB active agents for generating stimuli and a passive agent for checking the protocol and collecting coverage.

For example, if the module is a slave, then the UVC provides the active master, arbiter, and decoder that emulate AHB traffic on the bus. It also provides a passive slave for checking protocol compliance and collecting functional coverage.

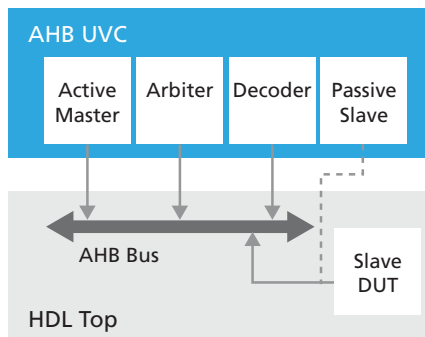


Figure 5: AHB UVC verifying a single slave

### Multiple AHB Module Verification

The AHB UVC can also verify multiple AHB modules of the same kind (for example, two masters) or of different kinds (for example, a master and a slave). Once again, the UVC provides the necessary agents for generating, checking, and collecting coverage.

For example, if the modules are an AHB slave and an AHB master, then the UVC provides the active arbiter and decoder

for generating stimuli, and a passive master and slave for checking and collecting coverage of the modules.

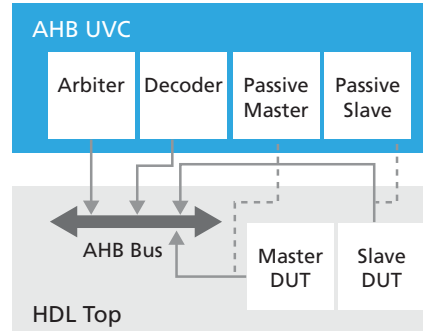


Figure 6: AHB UVC verifying a mix of masters and slaves

### Sub-Component Features

**Master:** burst attributes may be configured according to multiple parameters including:

- Kind
- Size
- Direction
- First address
- Lock and the list of transfers that can be controlled

**Slave:** response attributes may be configured according to multiple parameters including:

- Direction
- Data
- Address
- Transfer respond kind (OKAY, ERROR, SPLIT, or RETRY)
- Delay
- Split delay, number of split, and number of retry

**Arbiter:** responds to a transfer by withdrawing the grant from the master. The following parameters can be configured:

- Kind
- Transfer responses

**Decoder:** allows you to control the slave that is selected during reset.

### APB Master Verification

The APB UVC verifies the DUT by providing active slave agents for generating stimuli and passive master agents for checking the protocol and collecting coverage. Slave response attributes include:

- Transfer direction – read/write
- Respond delay
- Transfer respond
- Endianness – big/little

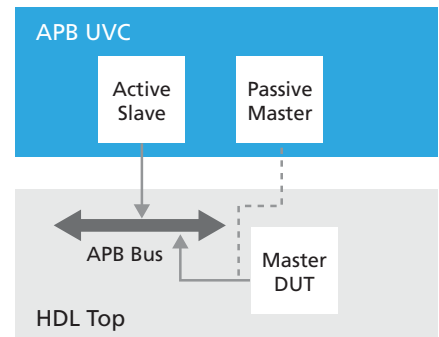


Figure 7: APB UVC verifying an APB master

### APB Slave Verification

The APB UVC verifies the DUT by providing active master agents for generating stimuli and passive slave agents for checking the protocol and collecting coverage. Master transfer attributes include:

- Address
- Data
- Directions

The APB UVC can also control the endianness.

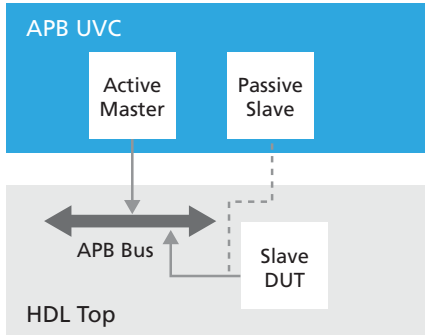


Figure 8: APB UVC verifying an APB slave

### Compliance Management System

The Compliance Management System (CMS) provides a protocol-specific, metric-driven verification environment that includes:

- An executable verification plan mapped to the protocol specification
- A library of constrained-random tests to isolate DUT corner cases
- An integrated coverage model to grade verification completeness
- Compliance checks and metrics to identify DUT verification gaps

### Protocol Compliance Using a vPlan and Test Suite

Protocol compliance starts with the verification plan (vPlan). All verification objectives are captured in the vPlan and correlated to the protocol specification on a paragraph-by-paragraph basis.

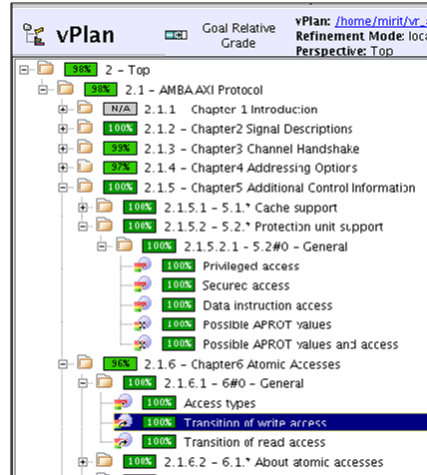


Figure 9: Section of an AXI vPlan indicating coverage for each AXI specification section

A library of constrained-random test sequences then stimulates the DUT with multiple parameter combinations for each coverage point of interest. This results in more exhaustive verification than running a large set of non-randomized validation tests.

Results from multiple simulation runs are integrated and graphically displayed in the vPlan window. Cumulative coverage vs. plan is displayed and any coverage gaps are clearly identified. The verification engineer then adjusts the test generation constraints to focus additional test sequences on the coverage points of interest.

Project management is facilitated through various reports and charts that measure progress against the plan. This provides early warning of schedule deviations and resource limitations.

### Learn More

A resource library plus support and training information are available at: [http://www.cadence.com/products/fv/verification\\_ip](http://www.cadence.com/products/fv/verification_ip).

Hands-on demos of Incisive verification IP are available at the Xuropa online community: [www.xuropa.com/cadence](http://www.xuropa.com/cadence)

Call 1.800.746.6223 to speak with a representative.

Grade	prev_write_access	write_access	Runs	Hits	At Least	Hits / At Least
100%	NORMAL	NORMAL	156	16405	10	1640
100%	NORMAL	EXCLUSIVE	57	954	10	95
100%	NORMAL	LOCKED	74	1045	10	104
100%	EXCLUSIVE	NORMAL	57	881	10	88
100%	EXCLUSIVE	EXCLUSIVE	72	6222	10	622
100%	EXCLUSIVE	LOCKED	20	86	10	8
100%	LOCKED	NORMAL	72	1122	10	112
100%	LOCKED	EXCLUSIVE	16	22	10	2
100%	LOCKED	LOCKED	75	2080	10	208

Figure 10: Results from a CMS test suite



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. [www.cadence.com](http://www.cadence.com)