

Encounter DFT Architect

Full-chip, synthesis-based, power-aware test architecture development

Cadence® Encounter® DFT Architect addresses and optimizes multiple design and manufacturing objectives—such as timing, area, wiring, and power—for today’s complex ICs and SoCs. Native to Encounter RTL Compiler, it offers a single, synthesis-based environment for developing high-quality power-aware test architectures that eliminate design iterations and reduce costs.

Encounter DFT Architect

Part of the Encounter Test family, Encounter DFT Architect is the industry’s first full-chip, synthesis-based, power-aware test architecture development product with top-down, bottom-up hierarchical design support. It is a key component of a true global synthesis environment where logic and design-for-test (DFT) constructs are compiled in a single pass for concurrent optimization of timing, area, wiring congestion, and power. This single environment—with advanced rule checking, structure verification, coverage optimization, and analysis—ensures the highest quality automated test pattern generation (ATPG)-ready netlist with an advanced full-chip test infrastructure.

Industry-leading power management techniques and testing of low-power functional modes make the combination of Encounter DFT Architect and Encounter True-Time ATPG the most robust, power-aware ATPG technology on the market. Integration with Encounter RTL Compiler global synthesis and the Common Power Format (CPF) allows users to create, insert, hierarchically connect, and verify test structures

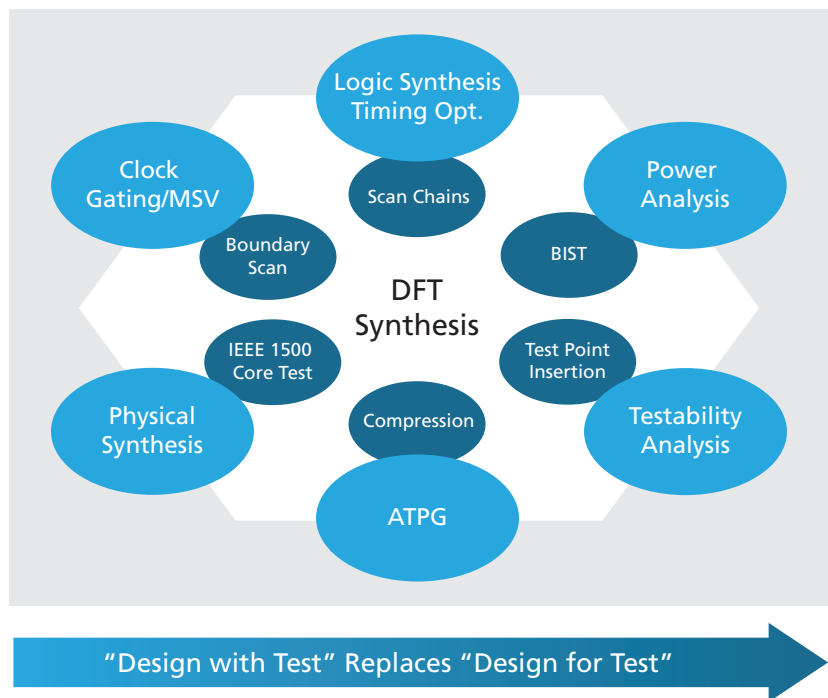


Figure 1: Native to Encounter RTL Compiler, DFT Architect is part of a single, integrated synthesis environment for ease-of-use and a one-pass flow

according to user specification. This unified methodology for “design-with-test” maximizes ease of use and accelerates the development of a higher-quality test infrastructure at lower cost.

Test architectures supported include full and partial scan, scalable compression (XOR and MISR), MBIST, LBIST, on-product clock generation

(OPCG), boundary scan (1149.1/6), I/O test, IEEE 1500 core wrapper, power-aware DFT, and power-aware ATPG.

A coverage optimization methodology ensures the highest fault coverage using highly efficient pattern sets. Automated shadow logic and test point insertion with links to ATPG facilitate optimization through random resistive fault analysis and deterministic fault analysis.

Low pin-count, high-throughput testing is enabled through the use of compression, ensuring the lowest tester cost potential including adoption of multi-site wafer test. Ultra-low pin-count SmartScan technology enables test for analog/mixed-signal designs with limited digital inputs. MBIST and LBIST can be accessed with either TAP or Direct-Access. Automated transition testing is now achieved through the specification and insertion of a programmable on-product clock generation (OPCG) macro. The user-defined OPCG is automatically inserted within Encounter RTL Compiler, which also generates the required protocol files for ATPG.

Encounter DFT Architect is available in two offerings: Basic and Advanced

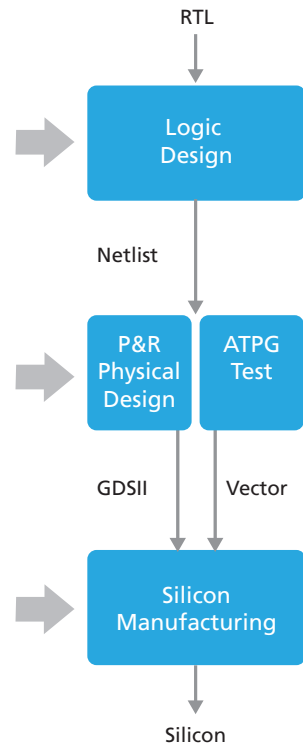
Benefits

- Performs concurrent logic and DFT synthesis across area, timing, wiring congestion, and power parameters
- Boosts productivity from RTL to ATPG by moving test decisions, structure verification, and analysis to the front end
- Accelerates development of a higher-quality IC test infrastructure for transition defect testing, including auto-generation and insertion of OPCG macros and ATPG protocol files
- Performs automatic IC test infrastructure insertion and verification from a single specification and environment
- Supports hierarchical and flat design flows
- Eliminates errors caused by manual stitching and integration

- SoC Test Infrastructure**
- Maximize productivity
 - Maximize predictability

- Test Pattern Generation**
- Maximize product quality
 - Minimize test costs

- Diagnostic**
- Maximize yield and ramp
 - Maximize silicon bring-up



- Encounter DFT Architect**
- Full-chip test infrastructure
 - Scan compression (XOR and MISR), BIST, IEEE1500, 1149.1/6
 - ATPG-aware insertion verification
 - Power-aware DFT and ATPG

- Encounter True-Time ATPG**
- Stuck-at, at-speed, and faster-than-at-speed testing
 - Design timing drives test timing
 - High-quality ATPG

- Encounter Diagnostics**
- Volume mode finds critical yield limiters
 - Precision mode locates root cause
 - Unsurpassed silicon bring-up precision

Figure 2: Encounter Test offers a complete RTL-to-silicon verification flow and methodologies that enable the highest quality IC devices at the lowest cost

- Power-aware DFT inserts specialized test control structures, and validates and tests all power modes
- Power-aware ATPG with early power estimation capabilities identify power issues during test mode and eliminate-costly iterations
- Performs physically-aware scan placement and ordering as well as test compression logic physical optimization
- Test coverage optimization enables early testability analysis and test point insertion to improve test pattern volume and test coverage
- Fully integrated MBIST solution optimizes memory test development time and reduces project costs
- Fully integrated LBIST solution with low area overhead and efficiency to decide tradeoff between runtime and coverage
- Flexible compression architectures (MISR, XOR, or hybrid) dramatically reduce manufacturing test cost, increase throughput, and optimize diagnostic flows

- Advanced masking architectures ensure the highest compression while maintaining full scan coverage

Encounter Test

Part of the Encounter digital design and implementation platform, the Encounter Test product family delivers an advanced silicon verification and yield learning system. Encounter Test comprises three product technologies:

- **Encounter DFT Architect:** ensures ease of use, productivity, and predictability in generating ATPG-ready netlists containing DFT structures, from the most basic to the most complex; available as an add-on option to Encounter RTL Compiler
- **Encounter True-Time ATPG:** ensures the fewest test escapes and the highest quality shipped silicon at the lowest development and production costs
- **Encounter Diagnostics:** delivers the most accurate volume and precision diagnostics capabilities to accelerate yield ramp and optimize device and fault modeling

Encounter Test also offers a flexible API using the PERL language to retrieve design data from its pervasive database. This unique capability allows you to customize reporting, trace connections in the design, and obtain information that might be helpful for debugging design issues or diagnostics.

Features

Encounter DFT Architect Basic

Encounter DFT Architect Basic includes all of the features required to create the basic test infrastructure for digital designs:

- A powerful schematic browser for control over what is displayed, how the circuit is displayed, how far tracing will go, and hierarchical navigation; a block can have its output nets traced, justified, and sensitized manually for easy debug and analysis
- Flexible, highly automated methodology for inserting all top-level test structures, including IEEE 1149.1/6 boundary scan controller, I/O test, and support for additional custom functions or variations
- Scan insertion with Encounter RTL Compiler global synthesis technology; required hierarchical connections to the TAP controller are addressed at the top level; designers can also use any industry-standard macro or IP for block-level scan insertion
- Full suite of ultra-fast checking, auto-repair, and analysis functions—including test structure verification, boundary scan conformance checking, and verification—allows cores to be isolated for SoC testing; schematic browser enables interactive analysis capabilities with simulation and fault analysis

Encounter DFT Architect Advanced

Encounter DFT Architect Advanced includes all of the features of the Basic configuration, plus XOR and MISR compression, LBI, and MBIST capabilities. The Advanced offering compiles and connects compression structures; tight links to Encounter True-Time ATPG Advanced technology enhance its capabilities. True-Time ATPG Advanced works with the inserted compression struc-

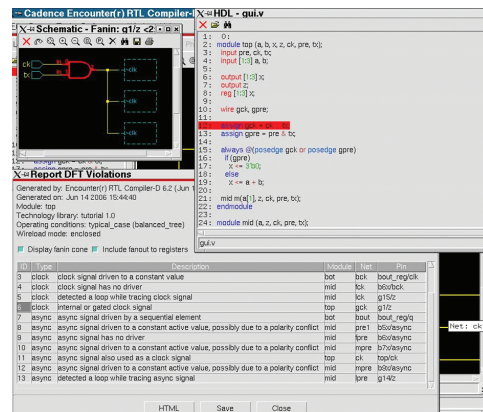


Figure 3: A single, fully integrated, synthesis-based environment with advanced ATPG DRC minimizes design iterations

tures to cut test costs and reduce scan test time and data volume by as much as or greater than 100x.

Encounter DFT Architect Advanced offers a highly flexible approach to compression. It enables the implementation of a multiple input signature register (MISR) architecture with the highest compression ratio, and the implementation of an exclusive-or (XOR)-based architecture for a highly efficient compression ratio and a one-pass diagnostics methodology.

- On-product MISR plus (OPMISR+) includes input fanout, broadcasting each scan pin to multiple scan-chain inputs, and MISR-based output compression, which eliminates the need to check the response at each cycle
- XOR-based compression includes input fanout (with the addition of an XOR-based spreading network) and XOR-tree-based output compression, which enables a one-pass diagnostics methodology
- Flexible and comprehensive masking algorithms for OPMISR and XOR compression strategies maintain full-scan fault coverage and the most efficient pattern and tester cycle count (e.g. wide0, wide1 masking); TAP-controlled, serialized compression meets or exceeds the lowest pin-count requirements

Problem:

- ATPG DRC run after synthesis
- Each violation requires a design change and synthesis re-run

Solution:

- Add ATPG checks to synthesis environment
- Enable identification and autofix capability early in flow
 - 3-state contention check on internal and external nets
 - Async set-reset race condition
 - Clock and data race condition
 - Floating nets
 - X-source checking

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- Support for asymmetric compression structure reduces pin requirements, enabling more pin sharing combinations, lower area overhead, and faster test time

Encounter DFT Architect Advanced also enables power-aware test, including power-aware DFT, ATPG, and analysis. Power-aware DFT supports low-power designs implementing a power shutoff (PSO) structure with the insertion of specialized test structures, such as a power test access mechanism (PTAM), that ensure stability of power domains during manufacturing test and allow users to set up different power modes for test. The automatic creation of test modes for each of these power modes enables verification of low-power intent and generation of power-safe patterns at the tester.

Information from the Common Power Format (CPF) is taken to compile and connect all low-power DFT structures into a complete, full-chip, low-power DFT infrastructure. Power-aware DFT enables a smooth path to advanced low-power ATPG, which generates tests for failures in low-power components such as state retention cells, isolation cells, and level shifters. Advanced fault modeling capabilities allow for defects in low-power components to be modeled accurately for ATPG and diagnostics.

After DFT insertion, each test mode is verified to assure power domain isolation, scan chain integrity for each configuration is checked, and the correct PSO logic

operations are confirmed. Encounter DFT Architect Advanced is fully interoperable with Encounter True-Time ATPG Advanced power-aware ATPG capabilities. Power-aware ATPG methods leverage advanced power management techniques to limit power consumption during manufacturing test.

Encounter DFT Architect Advanced employs selective clock gating and uses power-aware scan chains to further limit power consumption. Power is managed in scan shift and capture modes. The Advanced configuration also enables early estimation of scan power using accurate power numbers from library data. Power-aware ATPG helps prevent power consumption from exceeding chip power limits and eliminates costly netlist iterations toward power closure.

Integration with Encounter True-Time ATPG leverages intelligent ATPG algorithms to minimize scan correlation issues, delivering demonstrated results of >99.5 stuck-at test coverage with test time reduced by >100x. Optional X-state masking is available on a per-chain/per-cycle basis. Masking is usually required when using delay test because delay ATPG may generate unknown states in the circuit.

Encounter DFT Architect Advanced enables users to insert and connect custom structures such as an LBIST controller or an OPCG controller. In many high-speed applications, the design's on-product clock can be leveraged for test purposes, such as with Encounter True-Time ATPG clocking.

Encounter DFT Architect Advanced supports the specification and validation of the OPCG access points required by the ATPG engine.

- MBIST with robust fault coverage, easy BIST engine sharing, and automatic insertion and connection into hierarchical designs
- Support for embedded memory from leading suppliers
- Support for all common and required algorithms
- Failure analysis reporting from BIST diagnostic registers
- Row and/or column memory redundancy analysis

Encounter DFT Architect Advanced provides a simple and flexible LBIST solution with low area overhead, automatic insertion, and connection into hierarchical designs.

- Efficiency to decide tradeoff between runtime and coverage
- Flexible control interface with either JTAG or two pins LBIST control

Encounter Test offers a flexible API using the PERL language to retrieve design data from its pervasive database. This unique capability allows users to customize reporting, trace connections in the design, and obtain information that might be helpful for debugging design issues or diagnostics.

Platforms

- Sun Solaris (64-bit)
- HP-UX (64-bit)
- Linux (32-bit, 64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
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