CDNLive! EMEA, 25-27 June 2006, Nice, France

SystemC TLM for Complex IP’s verification

Laurent Ducousso - STMicroelectronics
2005 IP verification activity & status

Project Verification flow

SystemC TLM, IP verification history

A complex IP projects:
- Heterogeneous Architecture
- Strategy
- Environment
- Simulation environment
- Test generator’s
- Acceleration
- coverage
- Complex IP’s in HEG products

Future work
2005 IP verification activity & status

% bug
• bug = problem reported after
• IP verification completed

2005
40 IP's verified

11 SOC's integration

% of IP's (mm2)
2005 IP verification activity & status

40 IP's verified
11 SOC's integration

2005

% bug

• bug = problem reported after IP verification completed

% of IP’s (mm2)

0%
10%
20%
30%
40%
50%
60%
70%
80%
90%
100%

2003 2004 2005

tbv
specman
legacy

0%
20%
40%
60%
80%
100%

2003 2004 2005

tbv
specman
legacy

Legacy
Specman
SC TLM

L. Ducousso 8/2/2006
Project Verification flow

TB Approach
Run software in Target system
- System - level directed tests
  - C/C++

Model Abstraction
TLM
- Transaction-level Simulation

Engine
RTL
- Simulation
- System - level directed tests
  - C/C++

Full Chip
- Simulation & Acceleration

System
- Emulation

Run software in Target system
- System - level directed tests
  - C/C++

SysC/TLM
- Simulation &
  - Acceleration

SysC/TLM
- System - level directed tests
  - C/C++

SysC/TLM
- System - level directed tests
  - C/C++
SystemC TLM, IP verification history

<table>
<thead>
<tr>
<th>coverage</th>
<th>assertions</th>
<th>sceptman/CATG/e</th>
<th>Specman/CATG</th>
<th>SC TLM + BFM</th>
<th>PSL</th>
<th>SC/Xtreme</th>
<th>SCEMI-HTI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coemulation</td>
<td></td>
<td>Coware/Celaro</td>
<td></td>
<td></td>
<td></td>
<td>C/palladium 1</td>
<td>SC/palladium 2</td>
</tr>
<tr>
<td>Cosimulation</td>
<td></td>
<td>Specman/CATG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>scripts</td>
<td></td>
<td>RTLGUI/DM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>generation</td>
<td></td>
<td>Specman/C+e</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>reference</td>
<td></td>
<td>Coware</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDMPEG2</td>
<td>LCMPEG</td>
<td>DeltaPhi</td>
<td>DeltaMu</td>
<td>DeltaMu</td>
<td>DeltaMu</td>
<td>DeltaMu</td>
</tr>
</tbody>
</table>
**Multistandard HD video decoder, Graphic or Display processor**

**Heterogeneous Architecture**
- Software driver, ST40 @ 200Mhz
- Firmware, ST231 @ 400Mhz
- Firmware, slimcore @400Mhz
- Hardware, > 1Mgate @ 400Mhz
Verification Strategy

- HW block testing
  - Stimuli applied to design
- FW + HW co-verification
  - Norm or algorithm checking
- SW validation
  - Visual qualification of streams

**top-down verification**
- Only top level reference model exists
- Maintenance and devt of module env + ref model too costly

**hw/sw part constantly moving**
- Specs changing
- Requirements changing

**need to use simulation + emulation/acceleration to get through verification**
**Verification Environment**

- **RTL cores + hardware**
- **SystemC virtual SOC**
  - Host processor
  - System bus
  - System memory
  - On the fly timing randomisation
  - +Speed of txn implementation
  - -weak controllability/observability
- **Specman tests generation**
  - Pre-compiled tests
  - C verification driver
  - Memory input datas
  - + e langage capabilities
Test generator’s

- pre-generated tests
  - re-usable for sim and emulation/acceleration
  - due to top-down very directed tests with limited randomization
  - limited coverage on randomized sub-ranges
- Data randomization (AVP) decoupled from timing randomization (IVP)
Simulation platforms

- **Simulation platforms**
  - **Cosimulation RTL**
    - Specman tests (AVP, IVP%)
  - **Coemulation (BCA level)**
    - Specman tests (IVP)
    - Conformance streams (IVP)
  - **Coemulation (TXN level)**
    - Specman tests (AVP)
    - Conformance streams (AVP)
    - Code coverage
  - **SystemC (TLM tac level)**
    - All Expected results
  - **PSL**
    - Performances
    - Power management
    - Protocol
    - Security

**Simulation platforms Diagram**

- **CPU**
- **Memory**
- **TLM TAC**
- **Packetizer**
- **BFM adapter**
- **Packetizer**
- **BFM adapter**
- **Packetizer**
- **PSL assertion**
- **IP (RTL) Simulator**
- **IP (gates) Emulator**
- **BFM (gates)**
- **IP (TLM tac)**

- **JTAG**
- **Embedded SW debugger**

- **0.5kHz 30x 15kHz 280x 100kHz 12Mhz**
Xtreme Server Simulation Acceleration
Non Regression Environment

- Massive simulation parallelism deployment (16 jobs at a time automatically managed by lsf)
- More than 100k tests to run, more than 10k tests per day
- Environment managed by design team
- Works with Palladium as well

Video decoding, graphic or display testsuite

LSF
IP Coverage for testplan driven verification

Reference model coverage

- Code Coverage (GCOV)
- Mutation Coverage (CERTESS-Certitude)

Design implementation coverage

- Code Coverage (Xtreme + TransEda)
- Mutation Coverage (CERTESS-Certitude)

Model Abstraction

Engine

- Transaction-level Simulation
- Simulation
- Simulation & Acceleration
- Emulation

RTL

System

Block / Module

Cluster / Block

Full Chip

SysC ref model
World First for Sagem Communication and STMicroelectronics: First MPEG4 Set-Top Boxes Based on Single-Chip Video Decoder

Roll-out of leading-edge set-top boxes from Sagem, powered by ST’s STB7100 MPEG4 decoder chip, will enable broadcasters to offer increased number of digital TV channels.
IP verification : Future work

- Extend vertical reuse flow to Memory 2 SOC Interface IP’s
- Simulation Flow enhancement (10-20k testcases per day)
- Assertion deployment (performance, power mgt, security, …)
- Hw verification enhanced for multi app’s Firmware on complex IP’s
Annexes