BEST PRACTICES FOR HIGH SPEED DIGITAL PCB DESIGN

ABSTRACT REFERENCE NUMBER 24

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INTERNATIONAL CADENCE USERSGROUP CONFERENCE
September 13-16, 2004
Santa Clara, CA
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1. Executive Summary

Electronics miniaturization, nanometer silicon, multi-gigabit serial interfaces, mixed-signal devices, and system-level design are creating new challenges for the engineering community. Working with CAD tools to design state of the art high-speed digital circuits and printed circuit boards (PCBs) requires multiple trade-offs and an interdisciplinary design team to create a working design smarter, faster, less expensive, and more reliable. High-speed design requires using not only traditional physical rules, but also true electrical rules such as delay, impedance, and phase matching. Up-front analysis to develop optimum rules that enables constraint-driven layout (place and route) meets these high-speed design challenges and accelerates time to market. Signal speed, increasing power requirements, and the density of modern board designs have created major areas of growing concern. Complex issues related to timing, crosstalk, differential pairs, impedance control, termination (reflections, overshoot), power delivery, EMI, material properties for multigigabit applications, and successful multilayer routing are among the challenges. Most of these interrelated issues can no longer be addressed with traditional tools and design methodologies. Intent on providing leading-edge solutions to these problems, Cadence® has introduced new technology integrated in the Allegro® system interconnect platform to address high-speed digital circuit and PCB design. Some of the Allegro platform components are first-of-a-kind technologies, some involve silicon-package-board co-design technologies, and all are designed to increase engineering productivity and optimize the quality and performance of electronic products (see Figure 1).

![Figure 1: The Allegro System Interconnect Design Platform](image-url)
This paper focuses on the sub-system of high-speed digital PCB design and outlines an interdisciplinary and concurrent design methodology, enabled and supported by a comprehensive set of Cadence tools introduced as the Allegro system interconnect design platform. Built on a common database, it seamlessly provides interoperability of tools to enable cost efficient and concurrent design and analysis of electronic circuits and their board implementation. Design process flows, parameters and metrics are provided, which help with assessing and quantifying your specific design situations. In addition, Cadence offers services in this area with expertise based on many years of experience in a variety of industries. As a result of this combined methodology/platform approach, ideas can be turned into new products much faster and more efficiently, which has significant competitive advantages for the adopter of this approach.

2. The Problem

In today’s fast paced electronic design environment with increasing technical complexity nobody can afford to repeatedly spin PCB layouts before yielding a producible, reliable and cost effective production design and remain competitive. New and updated methodologies and tools are required to support the trend indicated in Figure 2. Higher clock speeds at faster driver rise and fall times along with growing net densities and an increasing number of constrained nets at decreasing supply voltages and increasing supply currents are the challenges designers are faced with.

![Figure 2: Trends in high speed design](image)

The complex challenges – ensuring signal integrity, reliable timing, behaved waveforms, acceptable levels of crosstalk, adequate power distribution, levels of EMI to meet global regulatory requirements, successful multilayer routing, cost effective technology, and shrinking time to market – can no longer be met with traditional tools and traditional design methodologies.
More Expensive Technologies (MCMs, Flip-Chip, GaAs...)

Figure 3: Qualitative Technology Choices for High-Speed Designs

3. Allegro System Interconnect Design Platform, the tool set for an efficient High Speed Digital Board Design and Verification Process

The “Board-Level High Speed Digital Design and Verification” process is introduced and used as an example to detail the flows and metrics related to designing world-class PCBs (Printed Circuit Boards) that primarily contain digital ICs (Integrated Circuits) and discrete components.

An “overall” flow (Figure 4) provides the orientation of this process to a world-class hardware development cycle. This process describes how to use analysis to understand and quantify design margins prior to physical implementation to ensure that electrical aspects of the system will work reliably at higher speeds (beyond the speed barrier).

Emphasis is placed on two essential sub-processes, which will be further detailed:

1) Up Front Concurrent Electrical/Physical Design

2) Constraint Driven PCB Layout and Verification

“Up Front Concurrent Electrical/Physical Design” is a new process describing extra steps required to extend standard PCB layout to higher speeds by utilizing up front concurrent analysis to develop implementation constraints through modeling and simulation. It achieves successful first pass implementations by analyzing the electrical performance of logical/mechanical choices during the design phase.

“Constraint Driven PCB Layout and Verification” is a well proven world-class process for the layout and verification of all types of PCBs. It has been very stable and automated for many years. Design checks are integrated and errors are rare. World-class in this domain means efficient execution and data transfer. In addition, this report also describes an electrical layout analysis process that is now commonly in use in top-tier companies.
These processes are recognized as world-class. For example, in the commercial marketplace, electronic designs have narrow market windows that cannot be missed (for example, get out the “talking Barbie” by Christmas). As such, there is constant pressure/emphasis to move analysis up front in the design cycle. “Virtual prototypes” are now becoming more common through the increased use of design simulation. This is replacing the empirically-driven design/prototyping/verification methods of the past, which were heavily dependent on manufacturing and fabrication steps to achieve a fast throughput time. However, working in this manner forces a design team to thoroughly explore the system-level implications of design choices, as provided and emphasized in the “Up Front Concurrent Electrical/Physical Design” process.

The industry at large agrees that transmitting signals above roughly 100 MHz on a PCB requires some changes in process and technology. A normal reaction is to jump the speed barrier by using more expensive technologies such as MCMs (Multi-Chip Module), flip-chip, or GaAs (Gallium Arsenide). However, it is important to note that commercial products have achieved higher speeds by changing the process only in order to maintain very low material cost using standard technologies.

This new process is much more dependent on up-front concurrent electrical/physical design analysis. This is particularly true when the same technologies are used as for the lower speed designs. Using this process, millions of Pentium-level machines have been shipped with almost the entire processor subsystem nets clocking at 100MHz and higher. (Note that these are not point-to-point connections, but typical bidirectional multipoint address/data busses.) The speeds to which lower cost technologies can be pushed vary. Point-to-point signal implementations are starting to hit high volume up to 1000MHz, while other configurations have been pushed well beyond 1000MHz.

Regardless of technology choices (more expensive or less expensive), Cadence believes that design teams can benefit by employing the “Up Front Concurrent Electrical/Physical Design” process on the right side of the “Speed Barrier” (Figure 3). Benefits include lower cost, easier access to materials in volume, reduced risk of first pass implementation success, and better understanding of design margins are causing greater yield in manufacturing, and greater design options.

At the top-level, the described High Speed Digital Design and Verification process flow takes the design from the “System/Board Partitioning” task through to “Production Hardware” (Figure 4).
A block-by-block description follows:

**System/Board Partitioning** – With mechanical and electrical specifications defined, the PCB design actually begins here. This is where one decides on critical BOM (Bill of Materials) components, size of boards, types of board technologies, and board-board or board-backplane connections.

**Up Front Concurrent Electrical/Physical Design** - or more precisely stated - Constraint Development through Simulation during Up Front Concurrent Electrical/Physical Design - This block will be detailed later in section 4.1, where key aspects of the concurrent electrical, logical and physical design tasks will be defined and coordinated.

**Pre-Layout Design** - At this point, the design moves to implementation and begins realization in physical hardware. A world-class process may choose a thorough review at this point, or use smaller iterative reviews during the design phase in order to avoid catching problems only at the end of the design cycle.

**Constraint Sets** - Mechanical and electrical constraints are derived, defined, reviewed and imbedded in the database to perform constraint driven physical layout.

**Constraint Driven PCB Layout and Verification** - Greater detail for this block will be given later in section 4.2.
Pre-Proto Sign-Off - Physical hardware will now be built, and this event would normally be accompanied by a review or sign-off step.

Prototype Fabrication and Assembly – This is a manufacturing step and should be performed using a production representative assembly line to pin point manufacturing related and potentially yield impacting issues at this early stage.

Physical Hardware Verification - Now hardware is back for testing and debugging. A world-class process would not have feedback to the design phase to correct errors at this point. However, a small percentage of boards (<20%) may find problems requiring a slight modification of the PCB layout (as shown by the dotted line). Other problems may be handled through “workarounds” in software or possibly hardware modifications. Hardware problems would be handled either at the assembly level or as a modification of the layout. Up until recently, a fair amount of electrical testing may have been done to correlate waveforms with simulation. As these tools/processes have matured, today’s world-class process would only verify a small sampling of signals using the appropriate test equipment (oscilloscope, VNA, …) to confirm they are performing as predicted through analysis. However, in the less mature area of multi-gigabit signaling, electrical testing and correlation with analysis results will be continuing as a means of gaining confidence in present and new tools/processes for this emerging area.

Pre-Production Design Review – This is a manufacturing-oriented hand off point.

3.1 Up Front Concurrent Electrical/Physical Design

The diagram in Figure 5 details the “Up Front Concurrent Electrical/Physical Design” process and is most easily understood in the color version. The concurrent nature of this process can be seen in the coordination of the ELECTRICAL tasks (shown in red), the LOGICAL tasks (shown in green), and the MECHANICAL tasks (shown in blue).

When does this process start? It is imperative that this process be in operation while ICs and mechanical aspects of the PCB are being considered. The process is ready to begin when electrical specifications are made and sufficient detail is available for the second row of tasks to be performed. As such, the appropriate state of the first row of blocks is described first, followed by the last row of blocks and finally the remaining task execution blocks:

Electrical Requirements - Sufficient detail is available on the speed of operation of the design, power distribution schema, EMI needs, technology used in the PCB and its target layer count and stack-up, and a definition/budget describing acceptable signal behavior.

IC Design - The IC design must have progressed to the state where 90% of the pins and their functions are defined. From this, preliminary timing target specifications could be derived for the I/O as well as the initial choices for the I/O drivers/receivers on the IC. Power requirements and worst case switching currents are known to plan for appropriate power distribution on board level.
Figure 5: Up Front Concurrent Electrical/Physical Design Process Flow

Preliminary Board-level Schematic - Must have sufficient detail to identify nets on which electrical performance is critical (such as clocks, high-speed busses, etc.) Major blocks/components must be defined in order to begin floor-planning. In addition, logical connections/interactions must be clear enough to derive board-level timings.

Mechanical/Thermal Requirements - Board size/shape is known. Considerations related to critical component height, thermal, and, if applicable, structural constraints (e.g. location of mechanical stiffeners), must be known to begin floor-planning.

Constrained Route Topologies - Defined for all nets identified as critical. Developed and optimized through extensive sweep analyses accounting for example for component and material tolerances and manufacturing process variations. These must be captured in a format where they can be effectively/efficiently communicated to PCB layout (Constraint Manager).

Pre-Layout System Timings - Must include complete mathematical descriptions of all system-level timing paths (such as RDY set up to CLK) and constraints (such as CLK hi time). IC timing portion should have timings confirmed from IC physical layout.

Final Schematics/Netlist - No more changes planned or expected.
Proposed Floor-plan - Main aspects of placement/orientations are derived/described and imbedded in data base.

The process ends when deliverables in the bottom row are complete and embedded in the data base.

Detailed Explanation of Task Execution Blocks in Flow:

I/O Selection - This cannot be done from an IC-centric view. I/O buffers must not only be selected for best IC timing performance, but also must be sanitized for system performance. Many times a strong buffer may show good performance in IC design tools, but have far worse system-level timing and EMI implications than a weaker buffer. Custom I/O designs may also be needed.

I/O Models - Once proposed I/Os are selected, models can be derived for PCB simulation. These models are normally in SPICE format and are either converted to behavioral level [IBIS (I/O Buffer Information Specification) or tool-dependent] or used directly, depending on the simulator. Validation of the selected/generated model is essential before this key step in high speed design is complete.

IC Timings - These timings are initially “targets” expressed in a preliminary specification. Throughout the process they will become sanitized by the logical implementation and later by the extracted physical layout of the IC.

Preliminary System Timings - This is a collection (typically a spreadsheet) of all the board/system-level timings. Generally, all paths are IC to IC and are either synchronous or asynchronous. Basic clock skew and performance parameters must also be collected and tracked. These logical/mathematical timing relationships should be organized into a format that can be easily saved, modified, and shared team-wide. The timing relationships must also include timing parameters for PCB signal propagation.

Identify Critical Nets - The preliminary schematics must be carefully examined to identify all physical connections that have either critical timing or performance parameters. This list is generated by looking at the design at a system level and is the key driver for the electrical analysis and pin-out process.

Preliminary Floor-plan – This is done by examining key components and their expected location/orientation on the PCB. Creating the preliminary floor-plan is most effectively done in a layout tool with a (very) preliminary net-list loaded of the key connections and initial IC pin-outs. At this stage it is advisable to perform a preliminary analysis of power plane pairs and decoupling capacitor selections and placements. Critical IC floor-planning locations, IC switching currents and power supply locations are key inputs for these simulations. Changes in capacitor selection and/or quantity will be used to update the schematic and any critical capacitor placement becomes part of the floor-plan.
PCB Simulation - This task collects key inputs from the electrical/logical/physical design processes and tests assumptions against various proposed physical instantiations. Simulations are transmission line level analog simulations, where the lengths of net segments are approximated based on the preliminary floor-plan. Power distribution simulations evaluate the grid based target source impedance values based on meshed plane pair models combined with models for decoupling capacitors and their placement locations. During this exploration phase, the development and optimization of constraints is performed through extensive sweep simulations to account for all known variations affecting the performance of the design.

Can Derive PCB Topology? - All topology simulation outputs must be judged against system-level timing constraints and electrical performance budgets (such as acceptable overshoot/ringing limits) to verify the feasibility of the proposed I/O drivers, timings, and physical placements. If acceptable, the key aspects of a functional topology must be captured for communication to physical layout. If not acceptable, see next step…

Concurrent Pre-Layout Multidisciplinary Solution Space - Failed topologies can normally be fixed in a variety of ways. It is a system-level decision to take the collective “path of least resistance” and impact either the I/O selection, IC timing, system timing, or floor-plan. If this process is run at the correct time during the hardware development cycle, all options are acceptable with an acceptable amount of negative impact.

Optimize IC Pin-out - Intelligent planning of IC pin-outs to comprehend PCB routing can normally yield savings in PCB layers as well as time required to complete an acceptable route. A carefully chosen pin-out can shorten critical signal lengths which can significantly improve signal transmission. The pin-out optimization process normally results in an iteration of the IC design, since not all available options satisfy the needs for either lead-frame, bonding, RDL (redistribution layer) routing, die bumping, power bussing, or other issues.

Mechanical/Logical/Electrical Requirements OK? - Check floor-plan against thermal/height/keep out/other requirements.

3.1.1 Process metrics

PCB designs with numerous nets faster than 100 MHz need to use the “Up Front Concurrent Electrical/Physical Design” process. Cadence has seen many cases where failure to do up-front analysis resulted in extra back-end design spins. Electrical signal problems are also much harder to find in physical hardware due to buried nets, logic complexity, and the difficulty of quickly/easily probing today’s fine pitch devices. Probe loading and associated changes in signal characteristic, is an additional aspect that needs to be taken into consideration. One extreme case involved five top engineers from three companies hunting for a problem that took four weeks to even identify as an electrical signal issue. After that time it took three more weeks to understand the cause of the problem, and then eight more weeks and 6 PCB spins (3 spins each of 2 boards) to correct it. At that point it was really more of a workaround as it would have been necessary to find the issue up-front in the design cycle to fix it correctly.
Using concurrent up-front analysis greatly increases the likelihood of getting good first-pass hardware. Analysis is not perfect in that sometimes phenomena occur that wouldn’t have been predicted or would have been too difficult to simulate. However, a significant amount of risk can be removed. The whole process requires a lot of expertise and judgment over the amount of design margin that is acceptable. Some design teams design with lots of margin - even up to 100%. However, in high-speed design this is normally not an option. For example, you wouldn’t expect to be able to get all the worst-case component timings in a 20nS path to add up to 10nS.

To orient the process measures stated in Table 1, an applicable “Baseline” design has been chosen. This is an 1200-net design with four new large 400 pin ICs integrated onto a 100 square inch FR4 (normal, low-cost PCB fiberglass construction material) PCB. The design has a fair amount (70%) of nets running at high speed (greater than 100 MHZ) and will reduce PCB layers to save cost.

Measures for “Time” and “Cost” in the table vary based on the “Variation Assumptions” listed under the DESIGN PARAMETERS. The “Variation Assumptions” are more subjective parameters, but have the most impact on changing productivity and throughput. “Newness of Design” refers to how similar this design is to previous ones. “Teamwork/Concurrency” is the degree to which the team functions as a unit. For example, when someone makes a change or assumption, do they know immediately who that will impact and discuss it with them? If they do, then the teamwork/concurrency is high. If not, the team finds out problems in larger “review” settings, takes longer to recover, and is much less efficient.

“Skill Level” is also a major variable in throughput time because engineers with less experience often get too distracted with the simulation tools, are slower to draw conclusions, and will tend to try more ineffective solutions before finding one that works. Working this process requires a fair amount of craftsmanship, expertise, and judgment, yet there is also a lot of time consuming computer use for setup and simulations. As such, the process is normally driven by someone with lots of experience who coordinates with engineers with less experience to perform the simulations. Ten years is a lot of experience in this domain, and utilizing engineers with more experience has significant impact on improving execution time.

This process would typically be worked by the following group of people: 2 engineers doing electrical simulation (1 primarily responsible for models), 1 engineer doing board-level design (including system timings, and interfacing with IC design), 0.5 engineer from IC design, 0.5 engineer from PCB layout, 0.5 engineer/technician for mechanical/miscellaneous.

This process applies to designs ranging in speed from roughly 8 MHz to approximately 2.5 GHz. The steps/skills/measures are basically the same, but the technology used would be changing. The lower frequencies could use CMOS in low cost packaging, moving to CMOS, ECL (Emitter Coupled Logic) and GaAs in more expensive packaging at the higher frequencies.
It should also be noted that the "*"s in the measures table call out generic process measures that are not meant to apply to the baseline design chosen. All other rows without "*"s work vertically in the table, and the baseline design assumptions define the reason for variation.

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NOTE: *denotes a generic process measure, i.e. does not refer to baseline design

Table 1: Process metrics
Notes description for line items in the Table 1:

“Efficiency” line items measured in “# iterations” refers to the number of revisions that might be expected for the given task. If the number is too small, the team may not be collecting input from the various disciplines. If the number is too large, the team may not be communicating effectively or be inexperienced.

In the case of “Optimize IC Pinout,” a large number of iterations and analysis may be required if there are cost/packaging reasons for trying to minimize the number of power and grounds. If so, there will be more iterations with minor changes (“shifting” of signal busses), that should not impact floor-planning progress.

Preparing simulation models is often the most difficult part of this process, and each project normally requires many new models. Some models can be found on the web, others can be purchased, others made from Spice simulation data, some derived from measurement. Whatever the case, time will be required to perform this task. “IBIS” format models are normally used in this process, although Spice models can also be used effectively if the task is not too large. More information about IBIS models is included in the “Electrical Verify” flow description in the “Analysis/Constraint Driven PCB Layout and Verification” section.

“Topology Derivation” is one of the key tasks. If floor-plan/pin-out is not optimized, there may not be a workable topology. Derivation of critical clock structures may take longer than others. Fortunately, when a good topology is found, there is a high probability it will work as simulated in actual hardware, as shown in the “First-pass yield on topology” row. “Topology” refers to route styles, line impedances, terminations, or anything else imposed at the board level to achieve signal integrity.

The average “Total Cycle Time” is one quarter (12 weeks), assuming the level of staffing listed in “Engineering Costs”. The primary parameter that would effect cycle time (other than those listed) would be the percentage of nets constrained (or, at speeds above 25 MHz). For designs with very few high-speed nets, this process may not be needed to its full extent. For very dense high-speed designs, more optimization/analysis would be required.

3.2 Constraint Driven PCB Layout and Verification

This process applies for all digital PCBs, high-speed or not. There are well-defined inputs and outputs to/from the PCB layout process

Inputs:

Schematic/net list, BOM (Bill of Materials), footprint mechanics, layer target/stack up, board mechanical (outline, connector placements, edge fingers, height restrictions, etc.), board thermal, route priorities, constraint set

Outputs (test/manufacturing related):
Photo plots/Gerber, drill tape, fabrication drawing, assembly drawing / instructions, solder masks, back-annotated schematics, final BOM, component locations for assembly, NC routing tape, net list for test

Figure 6: High Speed Digital PCB Layout process flow

The process flow outlined in Figure 6 represents a world-class PCB layout process.

A block by block description follows:

INPUTS – Typical inputs are listed above.

Make New Footprints - Before a placement/routing can begin, new devices that do not have a physical description (footprint) must be generated.

Preliminary Placement - All devices must be placed on the PCB outline, staying clear of keep-outs and mounting holes, to validate that the PCB size/shape is sufficient. Critical component
placement will be driven by constraints and must be handled accordingly. If all devices do not fit on top and bottom, the mechanical assumptions will have to be revised.

Routeability Analysis - With the netlist loaded and the ratsnest on, the placement (positions/orientations) is adjusted to simplify the route process by studying the basic flow/crossing of signals. Power planes and copper areas are studied along with decoupling capacitors and their placement.

90% Placement – Constraint driven placement is complete and nearly all placements can be locked in. However, some freedom to nudge components is desirable during the route phase to solve congestion problems that were not anticipated during the previous step.

Prioritized CONSTRAINT DRIVEN ROUTING - Regardless of the PCB being interactively or automatically routed, there will be some nets that need more attention than others. These nets may have certain restrictions defined by the design team. These restrictions must be documented in some way for clarity, and some routing systems allow them to be attached directly to the electronic database (but that is tool dependent). The Cadence ALLEGRO Platform has the constraints attached directly to the electronic database. This flow shows three stages of prioritized constraint driven routing, but there may be more. “Route Critical Nets” is the first stage. Nets in this class may even require special widths or gaps between them and adjacent traces. “Route Sensitive Nets” is the second tier of signals to be completed, after which “Finalize Placement” can occur. Now the layout engineer can “Route/Complete Remaining”, which involves finishing all routes, test points, power planes, and any other special requirements. DRCs (Design Rule Checks) would normally be flagged throughout this stage for physical and electrical constraint violations.

Silk-Screen/Test Preparation Cleanup - This task may still require slight movement of traces to ensure silk-screen readability (per company standard) and exact placement of test points for bed-of-nails tester.

Manufacturing Review – It is important to make sure sufficient assembly rules/details were implemented.

Verify DRC – This is the final check to ensure all DRCs (Design Rule Checks) are clean.

Back Annotate - Any part/pin changes are fed back to generate the final schematics.

Generate OUTPUTS – This is for PCB fabrication, as previously listed.

ECO (Engineering Change Order) Process - Not specifically shown here, but often the biggest challenge in executing the PCB layout is the request for changes. Changes are often not easily handled in this physically-oriented process, but some amount should be anticipated. It is essential that the layout process have a “point” person to intelligently interface with the design team to accept valid changes and fend off changes that can wait, be handled in another way, or do not need to be done.
The optional “Electrical Verify” interactive process is described now.

Note that each prioritized route stage is driven by constraints and feeds in and out of “Electrical Verify” process as shown.

The “Electrical Verify” (in red) is a post-route verification process that has become a standard part of routing high-speed PCBs. It is an emerging (10+ years old) process that world-class commercial companies are now using to verify PCB layout performance. This step is best done concurrently with placement and routing. It augments constraint driven placement and routing and its DRC feedback and places the design team in a better position to react to problems found. Simultaneous Switching Noise (SSN) simulations are conducted to verify power and ground bounce level meet requirements. If the route is not analyzed until it is completely finished, it becomes very difficult to make changes.

Constraint Set - Constraint sets drive the placement and routing process and are managed with the Allegro Constraint Manager tool. It is common to all high speed components of the ALLEGRO Platform. It provides real time feedback to the layout engineer on violations of constraints. Generally, timing allotted to the interconnect structure is a key criteria used to judge a good or bad route. However, other parameters such as impedance, overshoot, and many more may also be used.

Component IBIS Models - IBIS (I/O Buffer Information Specification, Electronics Industry Association/EIA-656) is the generally accepted format for behavioral models of component I/Os and packaging. Use of full transistor-level models at this stage would make full-board analysis too time consuming, but is an option where required.

Simulate PCB - Power/ground plane allocation and sufficient decoupling to meet target impedance requirements are typically verified before the route process starts. This step is advisable, as changes to plane shapes could impact the signal return path and hence signal routing. The IBIS models are meshed with the routed nets, as they are finished, to do batch simulations of the route groups. These simulations are judged against the required constraints. If acceptable, the next route stage can proceed. If not, the failed nets must be re-routed. Since these steps are normally implemented by different engineers, it is common for the route to continue prior to completing analysis. The main goal is to get feedback on the routes before too much more of the route is completed, as it becomes increasingly difficult to rip-up and re-route. Power/ground plane allocation and sufficient decoupling to meet target impedance requirements is verified before the route process starts. Checking of SI and EMI using the EMControl rules for those constraints that the layout DRC and Constraint Manager do not support is performed as well.

Crosstalk Check - Full-board simulation can also be run (again using IBIS models) to check for crosstalk. Here, it is important that all nets be in place to get an accurate understanding of the board’s crosstalk or coupling. This check has become increasingly more important in recent years as components move to finer pitch, PCB layers are minimized, busses become wider, edge speeds increase, and higher frequencies allow less time for signal settling. Though technology dependent, most crosstalk can be avoided by using strict x-y routing between
layers, and using the widest possible gaps (e.g. 15 mil) between traces. However, this is often not practical therefore crosstalk analysis tools are used. Further more, SSN simulations will aid in verifying that more specific crosstalk and power delivery requirements are met.

3.2.1 Layout Process Metrics

Table 2 lists performance measures given for a “Baseline” design. The incorporated variations describe three different difficulty levels for routing this 1200-net design.

<table>
<thead>
<tr>
<th>Definitions</th>
<th>PCB Layout</th>
<th>Unit</th>
<th>Low</th>
<th>Avg</th>
<th>High</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline for Design</td>
<td>Design Size</td>
<td># nets</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
<td></td>
</tr>
<tr>
<td>Design Size</td>
<td># connections</td>
<td></td>
<td>3600</td>
<td>3600</td>
<td>3600</td>
<td></td>
</tr>
<tr>
<td>PCB Size</td>
<td>sq. inches</td>
<td></td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>PCB Technology</td>
<td>dielectric</td>
<td></td>
<td>FR4</td>
<td>FR4</td>
<td>FR4</td>
<td></td>
</tr>
<tr>
<td>Variation Assumptions</td>
<td>Nets Constrained</td>
<td>%</td>
<td>5</td>
<td>70</td>
<td>70</td>
<td>Nets faster than 100 MHz</td>
</tr>
<tr>
<td>PCB Signal Layers</td>
<td>integer</td>
<td></td>
<td>6</td>
<td>4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Hand-routed Nets</td>
<td>%</td>
<td></td>
<td>15</td>
<td>85</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td>Skill Level</td>
<td>years exper.</td>
<td></td>
<td>3</td>
<td>4</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Cycle Time</td>
<td>Total Cycle Time</td>
<td>calendar weeks</td>
<td>2</td>
<td>5</td>
<td>8</td>
<td>Includes placement/footprint setup</td>
</tr>
<tr>
<td>Engineering Costs</td>
<td>Layout Cost</td>
<td>engineering weeks</td>
<td>3</td>
<td>7.5</td>
<td>12</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Layout Process metrics

“Low” Column - This PCB has plenty of available route layers with very few constrained nets. Therefore, most of its nets can be auto-routed making this PCB require only two weeks for completion.

“Avg” Column - This PCB needs careful attention on 70% of its nets, requiring it to be primarily hand-routed. Since a couple of extra route layers are allowed, this PCB requires five weeks for completion.

“High” Column - This PCB is allowed only the minimum of two signal layers for routing, requiring it to be almost entirely hand-routed. Again 70% of the nets are constrained, pushing this difficult design to eight weeks for completion.

“Layout Cost” - Routing cannot typically be done in parallel; however, sometimes dual-shifts are used. These boards assume one shift with one full-time person routing and one half-time person helping with footprints and interface with the design team.
“Skill Level” - Variations normally do not have significant impact on execution time for PCB layout. An engineer with five years experience is very experienced, and significant gains are not achieved by utilizing people with more experience. The people with more experience normally just do a better job of interfacing with the design team and the manufacturing process to ensure that errors do not occur due to miscommunication.

3.2.2 Examples of PCB Layout Complexity

The line items in Table 3 describe the range of measures that might be encountered in various PCB layouts.

Layout density versus the number of layers used is the primary driver for complexity and schedule. Extra layers is also a good solution (although more expensive) for solving electrical complexity. Most items are self-explanatory. However, two are worth commenting:

Adder for Electrical Verify - When performed, the electrical verify process can only lengthen the layout task due to extra interaction and possible changes. A team that is working well may be able to contain the extra time to only one week, assuming the up-front routing rules and constraints were clear and verification is concurrent with routing.

First Pass Yield - PCB layout is a very stable process, with many checks built in making first pass yields very common (on the fabrication database generation, not the fabrication process).

<table>
<thead>
<tr>
<th>QUALITY</th>
<th>Complexity</th>
<th>Layout density</th>
<th>pins/in²</th>
<th>10</th>
<th>40</th>
<th>350</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Size</td>
<td>nets</td>
<td>20</td>
<td>1k</td>
<td>15k</td>
<td>could go higher</td>
<td></td>
</tr>
<tr>
<td>Via Drill Size</td>
<td>mils</td>
<td>12</td>
<td>16</td>
<td>27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trace Width / Space</td>
<td>mils</td>
<td>4 on 4</td>
<td>8 on 8</td>
<td>12 on 12 greater xtalk risk below 10 mil spacing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB Layers</td>
<td># layers</td>
<td>4</td>
<td>8</td>
<td>40+</td>
<td>could go higher</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Efficiency of Process</th>
<th>Layout Productivity</th>
<th>nets/week</th>
<th>100</th>
<th>200</th>
<th>400</th>
<th>Hand-route</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layout Productivity</td>
<td>nets/day</td>
<td>1000</td>
<td>2500</td>
<td>5000</td>
<td></td>
<td>Auto-route</td>
</tr>
<tr>
<td>Layout re-use (cut/paste)</td>
<td>hours</td>
<td>0.1</td>
<td>0.5</td>
<td>2</td>
<td>need netlist equivalence to be efficient</td>
<td></td>
</tr>
<tr>
<td>Footprint re-use</td>
<td>%</td>
<td>20</td>
<td>70</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>First Pass Yield</td>
<td>%</td>
<td>80</td>
<td>90</td>
<td>100</td>
<td>processes stable, failures due to miscom.</td>
<td></td>
</tr>
<tr>
<td>Number of iterations</td>
<td>integer</td>
<td>1</td>
<td>3</td>
<td>7</td>
<td>spins caused by changes/miscommunication</td>
<td></td>
</tr>
<tr>
<td>PCB Sim for Timing</td>
<td>nets/hour</td>
<td>50</td>
<td>200</td>
<td>400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB Sim for Crosstalk</td>
<td>nets/hour</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TIME</th>
<th>Cycle Time</th>
<th>Total Cycle Time</th>
<th>calendar weeks</th>
<th>1</th>
<th>4</th>
<th>12</th>
<th>Includes setup - mostly hand route</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Cycle Time</td>
<td>calendar days</td>
<td>0.5</td>
<td>1</td>
<td>3</td>
<td>98% auto-route assumed, no setup</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adder for Electrical Verify</td>
<td>calendar weeks</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Flexibility     | Outline / Placement | calendar days | 2 | 4 | 10 |                                             |
| Footprint creation | hours/component | 0.25          | 0.5 | 2 |                                           |

| COST            | Cost of errors     | Cost of Design Errors | $/spin | $500 | $2k | $5k | doesn't include opportunity cost |

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Table 3: PCB Complexity Range Examples

3.3 Sources of Data

Up Front Concurrent Electrical/Physical Design

Computer industry (sample size: 10), strong area within Cadence, data derived/verified by Cadence personnel who have put in place and managed groups to perform this task at leading commercial computer companies.

Constraint Driven PCB Layout and Verification:

Computer industry (6+), Industrial automation (1), Networking industry (5+), Service bureaus (4), another strong area within Cadence due to our large market share of design software in this domain - data was verified by layout experts within Cadence with over 400 years of collective experience.
4.0 Process Metrics with Maturity Level Definitions

A summary of process categories and their respective maturity levels 0 through 3 are defined in Figure 7.

This information is used in Figure 8 to visualize a “world-class” rated process opposed to a “typical” rated process of how a significant part of the industry is approaching Digital High Speed PCB Design, even today.
### Design Analysis Approach
- **0**: rule of thumb based past experience, no analysis
- **1**: some pre-route modeling and SPICE analysis
- **2**: pre-route and post-route point checking
- **3**: pre-route optimization and post-route batch analysis, automated data transfer

### Integration with Logic Simulation
- **0**: isolated environment, no interaction
- **1**: isolated environments, no interaction
- **2**: integrated via timing paths and spreadsheets
- **3**: fully integrated analog/digital simulation

### Design Concurrency
- **0**: no concurrency, some local optimization only
- **1**: some concurrency with local optimizations
- **2**: electrical & mechanical design concurrent (no component or IC)
- **3**: electrical, mechanical, logical and IC aspects developed & optimized concurrently

### Layout Constraints
- **0**: historically grown, based on experience, not analytically developed
- **1**: analytically developed, passed to layout in document/diagrams
- **2**: analytically developed, iterated, passed electronically with database
- **3**: automatically derived and attached to database

### Route/Analysis Integration
- **0**: rules approach, visually checked
- **1**: automated post-route check
- **2**: interactive hand-layout checking
- **3**: interactive auto-route checking

### Technology Selection
- **0**: stay below 1 GHz
- **1**: contain high-speed interfaces inside ICs
- **2**: address performance needs with expensive technologies
- **3**: achieve performance requirements with appropriate mix of design process & simpler, more accessible technologies

### Team Structure
- **0**: ad hoc and as needed staffing, no team
- **1**: organization functional rather than project focused
- **2**: multi-disciplinary teams in place, do not quite achieve concurrent process
- **3**: multi-disciplinary team implements concurrent process

### Crosstalk Analysis
- **0**: example scenarios in SPICE
- **1**: extracted board-level, estimated coupling
- **2**: full board extracted and simulated
- **3**: full board/system extraction, timing qualified

### Dependence on Empirical Analysis
- **0**: empirical used as only approach to understand/solve problems
- **1**: empirical approach combined with some (~10%) post-HW analysis used to understand/solve problems
- **2**: equal shares (50/50) mix of pre/post-HW analysis
- **3**: 95% replaced by pre-HW design analysis on projects, only used to validate brand new technology

### Model Development
- **0**: no ability to create or obtain, bound by purchased library
- **1**: no ability to create, but source obtained/working
- **2**: manual cut/paste from SPICE & datasheets
- **3**: automated generation from HW and/or SW

---

**Figure 7: Process Categories and Maturity Level Definitions**
5. Conclusion

High-speed designs require the true use of electrical rules in addition to physical rules to meet all of the demands of high-speed designs. With the Allegro System Interconnect Design Platform Cadence has introduced a design environment, which enables design teams to efficiently meet technical and economically driven time to market challenges associated with High Speed and Multi-Gigabit Designs. Up front concurrent electrical/physical design leads to constraint-driven placement and routing, which optimizes the design according to electrical rules while still obeying physical rules to meet manufacturing requirements. It adjusts the length to correct circuit delay, and spaces traces to achieve actual crosstalk limits. It automatically manages the implementation parameters to achieve electrically correct differential pair routing. It helps to optimize usage of decoupling capacitors and accounts for loop inductance with an understanding of loop area. Constraint-driven routing helps you create more robust designs by optimizing the layout with respect to timing and noise. This method reduces route-and-verify iterations, which ultimately speeds your time to market.
Combining the Allegro System Interconnect Design Platform and the “Up Front Electrical/Physical Design” and “Constraint Driven PCB Layout and Verification” sub-processes, will help to move your team to elevated productivity levels. The included “World-Class” process metrics and process assessment spider charts are intended to guide you in determining the economical benefits for your team and organization. Also, Cadence experts are available to partner with you in this endeavor.
Appendix

With the Allegro System Interconnect Design Platform Cadence Integrates the Flow for High-Speed Design

Highly complex, highly constraint PCB systems demand integrated, sophisticated design solutions. The Cadence PCB design environment is optimized for high-speed design and includes a number of industry-leading capabilities including the first, fully integrated constrain management system, a robust, common database that ensures data integrity throughout the design process. It is the industry’s first PCB design Platform system to offer users the flexibility to transparently operate on UNIX, Windows, or Linux platforms.

Fully integrated, the Allegro Platform design environment includes library creation and management, design entry, virtual prototyping and analysis of the interconnect structures, including power delivery design and analysis, electrical constraint management, and a powerful auto-interactive design tool. All of which are designed to move products from design into volume production quickly and reliably.

Co-Design Methods reduce cost and time to market

Faced with fast system-on-chip (SOC) or system-in-package (SiP), a package with thousands of I/Os, a complex multi-layer board, and a rapidly closing market window, engineers are eager to look across design domains for time and cost savings. Working with our partners and customers, Cadence has developed a number of technologies that support co-design methodologies. They represent some of the most exciting technologies in PCB system design today.

Silicon Design-In Kits solve new device design dilemmas

Implementing a new generation high-speed device into a PCB system is a time-consuming, challenging and costly process. Because PCB and IC design environments are so different, SPICE (IC) models must be translated to IBIS or behavioral (PCB) models in a lengthy and error-prone process. To address this issue, a new capability in Allegro PCB SI allows IC manufacturer to create IBIS model from SPICE, as well as silicon-design-in kits that enable PCB systems designer to drastically reduce implementation times for new designs. A design-in kit is an electronic blueprint for simulating and implementing silicon devices in a system and as such speeds time-to-volume production for the IC manufacturer and time to market for the system companies.

Complete Differential Signal Design Solution speeds network applications

Today complex multi-board network and communications applications can have hundreds – or even thousands – of differential signal pairs, causing long design cycles as engineers perform numerous “layout-simulate-fix” iterations to successfully complete a design. The new Cadence integrated differential signaling design solution allows engineers to create, constrain, simulate and manage differential signals throughout the entire design flow, addressing the problems
inherent in integrating nanometer-scale devices into systems with multi-gigabit serial interfaces.

**Concurrent IC Packaging and PCB Design**

Cadence continues to advance its IC packaging suites with concurrent design methods. Advanced Package SI uses a convergent methodology that considers the path from the silicon-to-package, package-to-board, and back to silicon, ensuring signal integrity across the interconnect structures. Plus, as the majority of IC packaging foundries use Cadence design technologies, both IC packaging engineers and systems designers can co-design and analyze the die-to-die interconnect, helping to ensure package cost and performance are optimized in the entire system.

**Signaling at Multi-Gigabit**

Cadence PCB technologies are used to design today’s and tomorrow’s leading-edge high-speed products. Utilizing Cadence products to their fullest extent, not only allows engineers and designers to meet the challenges of high-speed board designs, but also do it with unprecedented speed and accuracy, resulting in cost effective and competitive products meeting the market demands for quality and reliability.

**For more detailed information, please visit**


**BIOGRAPHY**

Juergen Flamm graduated from the “University Fridericiana” in Karlsruhe (Germany) with a MS EE in electrical engineering.

He gained his experience and expertise working in the industry at almost every possible level of engineering responsibility.

Early in 2001 he joined Cadence as a Pre Sales Field Application Engineer for SPB products with focus on the Allegro PCB SI family of high speed design tools.

He holds 5 patents in the areas of performance electronics and signal processing for fiber optic and MEMS sensors.