Designing Out DFM Issues at 65nm

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27th June 2006
Introduction

- Overview of S3
- What is DFM?
- Why DFM is an issue now?
- How can we improve our designs for DFM?
- Conclusions
About S3

- **Consumer Electronics Design Company**
  - Home Entertainment
  - Mobile Multimedia
  - Healthcare

- **Integrated Circuits and Embedded Software Solutions**
  - Worldwide Client Base

- **Unique Combination of Software and IP**
  - Single-chip, Power-efficient Systems

- **Getting Clients to Market Faster**
  - Expertise, Innovation, Products, Process
S3 - Nanometer Leadership

- **Global Leader in Nanometer IC Design**
  - On schedule right first time silicon
  - Mixed Analog / Digital SoC Focus
  - Over 25 Designs in 90nm
  - Developing in 65nm since 2004

- **Serving Top Tier Clients**
  - Including Atmel, Philips, Micronas
    Texas Instruments, Toshiba

- **Teaming with Leading Technology Partners**
  - Including Cadence, IBM, Synopsys, TSMC
What is DFM?

- Yield quantifies successful silicon die throughput
- DfM / DfY tackles known yield issues by best design practice
- Yield implication for unit cost:

\[
$unit = \frac{\$wafer}{(#die) \times yield} + test\_time \times ($tester)
\]

- Ultimately impacts the ROI for the IC vendor
- Trend getting worse for 65 / 45nm

- 90nm feature size created by 193nm lithography
  - “Like painting a thin line with a thick brush”

- Best design practice captured by working at leading edge technologies
Types of Yield Loss?

- **Random**
  - Particle Defects
  - Interconnect width

- **Systematic**
  - Feature Limited
  - Poly gate extension

- **Parametric**
  - Device Physics
  - Matching devices
Why is DFM an issue now at 65nm?

Drawn in Layout tool

Manufactured at older technology nodes

Manufactured at 65nm
How Can We Improve Our Designs For DFM?

- Design: Redundancy, testability, libraries, IP, etc.
- Layout: Robust layout: Library / re-usable IP, foundry yield analysis
- Review: Maturity consideration
- Manufacture
- Test: Failure mechanism analysis
DFM Aware Design Flow

- **Synthesis** (RTL Compiler)
- **Place & Route** (PKS, NanoRoute)
- **Floorplan** (SOC Encounter)
- **Routing** (Fire&Ice)
- **Physical Verification** (Third Party)
- **Formal Verification** (Conformal, Third Party)
- **Test Insertion** (DfT-Compiler)
- **Signal & Power Integrity** (CeltIC, VoltageStorm)
- **Chip-Finishing**
- **Chip Extraction** (Fire&Ice)
- **Physical Verification** (Third Party)
- **Floorplan** (SOC Encounter)
- **Synthesis** (RTL Compiler)

**GDS 2**
DFM Aware Power Grid

Non DFM aware

DFM aware
S3 Approach

- Even VDD / VSS grid
- Conditional spacing
- Wide track minimisation
Via Doubling

- **Risk**
  - High resistivity on single vias

- **Identify single vias on critical nets**
  - e.g. With respect to timing or matching

- **Doubling vias reduces faults**
  - 50% probability reduction

- **Post-route doubling**
  - Don’t compromise area
### S3 Approach

#### Pre multi-cut via insertion:

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#### Post multi-cut via insertion:

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Wire Spreading

Metal particle causing a short
**S3 Approach**

**Wire Spreading:**
- Avoids congestion
- Benefits both DFM and SI

**S3 Strategy**
- Use SOC Encounter SI awareness switches
- Route clock nets, top level nets and sensitive signals on double spacing
Conclusions

- Early in the Design Phase
- Foundry/Designer Collaboration
- Better Solutions for DFM from EDA Vendors
- DFM is a Business Opportunity
  - 5% increase in yield is worth $50M over the life of a cell phone
Visit S3 at Stand #05 or www.s3group.com for more information on our leading edge SoC Design capabilities and silicon proven 90nm Mixed Signal IP