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Application Note: S-Parameter Model Generation from Physical Layout Using Allegro PCB SI 630

The purpose of this application note is to describe the recommended process for extracting accurate S-Parameters for a differential pair from an Allegro physical layout using the Cadence Allegro PCB SI 630 toolset.

You will benefit from this application note if you:

- Are a SI engineer with some experience using the Allegro PCB SI 630 toolset
- Have access to licensed installations of Allegro PCB SI 630, versions 15.5 or higher
- Have access to the Allegro layout databases containing the signals you wish to model

Related information on this subject includes:

*Guidelines for Robust S-Parameter Model Development Application Note*, available from Cadence on Sourcelink.

**Overview**

The procedure described in this application note begins with the Allegro layout database for the signals of interest. The balance is organized into the following sections:

- Setting up material and stack-up data
- Extracting topology into SigXplorer
- Upgrading via models
- Defining ports
- Setting frequency parameters
- Generating S-parameters
Set Up Material and Stack-up Data

This step is included on the assumption that you, the SI engineer, have not received from the layout designer the appropriate material and stack-up information properly set up in the Allegro database. If such is the case, this is a crucial step, because any frequency or time domain analysis that follows it is focused largely on analyzing the effects of the interconnect parasitics in the layout. These parasitics are obviously directly dependent on accurate material and stack-up data. The best source of this information is the PCB fabricator. You need to know the specific stack-up that they will use, and the geometries and material properties checked against the cross section definition in Allegro PCB SI. The layout cross section (Figure 1) is invoked by choosing Setup > Cross Section in the tool's menu bar.

All the data in this form is important, but the critical items to check against the fabricator data is:

- copper and dielectric thicknesses
- dielectric constants
- loss tangents
**Note:** For conventional PCBs, the copper thickness of the TOP and BOTTOM layers should also include plating thickness, which typically adds about 1.2 mils or more to the copper cladding thickness.

Another important aspect is the dielectric constant associated with conductor layers. This represents the characteristics of the prepreg resin that flows around the metal conductors, and can sometimes be less than the composite dielectric constant of the core or prepreg material itself. For fine pitch differential pair geometries, this can have a significant effect on the characteristic impedance of the geometry.
Extract the Topology into SigXplorer

Once the stack-up data is correct, your next step is to extract the diff pair into SigXplorer, where you can generate S-parameters. Before extracting them, check how the preferences are set for modeling routed interconnect.

1. Choose *Analyze – SI/EMI Sim – Preferences* from the PCB SI menu bar.
2. Click the Interconnect Models tab, and review the settings in the Routed Interconnect Models section.

![Figure -2 Analysis Preferences Dialog Box](image-url)
For multi-gigahertz (MGH) applications, you should set a non-zero Cutoff Frequency, such as 10GHz. This will enable the field solver to model frequency-dependent skin effect and dielectric loss, which is crucial for these signals. The other important fields in this section to look at are **Diffpair Coupling Window** and **Min Coupled Length**. These parameters control how diff pair coupling is modeled in the topology. **Diffpair Coupling Window** controls how far apart diff pair traces can be and still be considered for intra-pair coupling. Likewise, **Min Coupled Length** controls how long a coupled segment must be to be represented as a coupled segment in the topology.

In the Topology Extraction section, toggle on **Differential Extraction Mode** to enable the coupled diff pair to be extracted. Also turn on **Diffpair Topology Simplification** to start with. Then go through the rest of the extraction process and review the resultant topology in SigXplorer. If more–or less–detail is desired, you can then modify these parameters and re-extract the diff pair. You can then repeat this interactive loop until the desired level of detail in the topology is produced.

Once the preferences are set up, you can perform the actual extraction from the Probe dialog box in Allegro PCB SI.

1. Choose **Analyze > SI/EMI Sim > Probe**.
2. Click on one of the diff pair nets in the layout to populate the form, then click **View Topology**.

**Figure -3  Probe Dialog Box**

If the SI models (associating diff pair pins together) and diff pair properties are set up properly in the database, this step is straightforward. If SI models are absent, we recommend that you verify that the nets are identified as a DIFF_PAIR in the database, and extract based on that information.

To determine if the signals of interest are tagged as part of a diff pair:

1. Choose **Display – Element** in the PCB SI menu bar.
2. In the Find Filter, click **All Off**, then check **Nets**
3. In the palette area of the UI, click on the net.

The Show Element window will appear. If the net is defined as a diff pair, it will be described at the bottom of the window. For example:

Member of Groups:

DIFF_PAIR  : DIF1_F2S1C1L1_RX

4. If the net has not been set up as a diff pair, choose Logic > Assign Differential Pair and do so. (See the on-line Help for the Assign Differential Pair dialog box if you are unfamiliar with how to set up the nets as diff pairs.)

Once defined as a diff pair, you can extract the differential topology if the environment is set up properly.

1. Choose Setup > User Preferences.

The User Preferences Editor appears, as shown in Figure 4.
2. In the Categories section on the left, click on *Signal_analysis*. Verify that *sq_enable_udiff_extraction* is turned on, as shown above. This enables you to extract diff pairs based on being tagged as part of DIFF_PAIR, and does not require SI models to be present.

3. Click *OK* to immediately enable this environment variable.

To perform extraction, a driver and receiver pin must be found on the net. You can determine this by looking at the Probe form after selecting one of the diff pair nets. Again, if SI models are set up properly, this should be all set. If SI models have not been set up, then you should define two drivers and two receivers for the diff pair.

1. Choose *Logic > Pin Type*.

   The Logic - Pin Type dialog box appears.
2. Click on the pins in the layout displayed in the palette of the UI.

   They become displayed in the Pin Type Assignment section of the dialog box, as shown in Figure 5.

3. From the New Pin Type drop-down, set two of the pins as type OUT and two of the pins as type IN.

4. Re-select the diff pair in the Probe form. You should see these pins appear in the appropriate columns of the form. At this point you can extract the diff pair into SigXplorer.
When you are building topologies that span multiple Allegro layouts (for example, two line cards plugged into a backplane), there are two ways to approach it. If connector models and DesignLinks have been set up to link the multiple layouts together, the full topology will be extracted automatically into SigXplorer. If this has not been done, it is possible to extract topologies from each of the layouts, and combine them together in SigXplorer with the File – Append command. Then all the topologies will appear in the same SigXplorer canvas, and they can be wired together, with connector models inserted.
Upgrade the Via Models

Once your topology has been assembled in SigXplorer, you need to upgrade the via models. Topology extraction utilizes the traditional closed-form via models from Allegro PCB SI, which are inadequate for multi-gigahertz (MGH) frequencies. These extracted vias should be considered “placeholders”, and you must replace them with via models from the Via Model Generator (VMG) in SigXplorer (or from external 3D engines).

**Note:** The Via Model Generation dialog box is accessed in the following manner:

1. Choose *Analyze – Libraries* from the SigXplorer menu bar.
   The Signal Analysis Library Browser appears.

2. In the Interconnect Library Files list box, select the interconnect library containing the via model to be upgraded and click *Browse Models*.
   The Model Browser dialog box appears containing a listing of the selected interconnect library.

3. Select the via model to be edited, and click *Edit*.
   The Via Model Generator Dialog Box appears.

Through-hole pins, such as those commonly used for backplane connectors, are ignored by the Allegro PCB SI > SigXplorer extraction process. They must be modeled in the same manner as vias, and added to the topology.

Coupled vias can be modeled in the VMG. This coupling should be included in the model for accuracy. Within the VMG, either the coupled signal vias (for example, for a diff pair), or one signal via and multiple equidistant ground vias, can be modeled. You should examine the specific layout to determine which type of coupled via model is most applicable.

**Note:** You must also account for backdrilling when generating via models. The Begin Layer and End Layer define the “span” of the barrel via. For example, the scenario shown in Figure 7 is for a 20-layer backplane. It is backdrilled from layer 20 through layer 11, so the Begin and End Layer parameters have been adjusted to limit the via barrel to exist only from layers 1 through 10.
When generating coupled via models (represented in S-parameter format), you must specify the Start Frequency, End Frequency, and Number of Frequency Points. (You make these settings in the Modeling Options tab of the Via Model Generator dialog box.) If you expect the via models to be used in time domain simulation, use care when selecting these parameters. Recommendations for these settings are:

Start Frequency – 10MHz

End Frequency – 2/t_rise

# of Frequency Points - 128
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As via models by themselves tend to produce S-parameters that are typically fairly smooth in nature, 128 points is usually sufficient. Increasing this value typically does not improve accuracy, and increases model generation times significantly.

When wiring up coupled via models into the topology, use care to ensure that the correct terminals are used. Note in the example shown in Figure 8 how the terminals of the connector model (ESPICE black box) are connected to the TOP layer terminals of the coupled via models.

Figure -8 Connector Models in SigXplorer
Define Ports

To examine serial data link topologies, we recommend that you place terminals at the positive and negative terminals of the driver and receiver, and generate a 4-port S-parameter model for the whole link, as shown in Figure 9.

Figure -9  Terminal Placement in SigXplorer (detail)

If you want to generate S-parameters for some portion of a topology, you must isolate the specific portion from the rest of the topology. You can do this in one of two ways:

Delete the unwanted sections from the topology, leaving the portion of interest

—or—

Use large (for example, 1meg Ohm) resistors to isolate the desired portion.

Failure to do this will result in unwanted sections of the topology being “sucked into” the resulting S-Parameter black box, resulting in undesired results. For example, assume the 4 ports were placed to encompass elements SL12, SL9, and SL11 as shown in Figure 10.
The resulting S-parameters would then also include SL14, SL10, SL13, SL15, and SL16, although external ports are not provided for them. Hence, they would be “hidden” in the S-Parameter model, essentially creating long unterminated transmission lines and producing excessive (and possibly unexpected) return losses.
Set Frequency Parameters

Before generating S-parameters, you should appropriately set the frequency parameters. For simply viewing the frequency response, these settings are not overly critical. In the S-Parameter Generation dialog box, simply set the Start Frequency and End Frequency for the range of interest. The Number of Frequency Points controls the granularity of the resulting S-Parameter plot, and can be adjusted as desired. Using 512 points is often sufficient to display most results with reasonable resolution, and is usually a good trade-off from a performance standpoint.

When generating S-parameters for use in time domain simulations, exercise much greater care in order to produce robust results. Recommendations for this are given in Guidelines for Robust S-Parameter Model Development Application Note, available from Cadence on Sourcelink.

Generate S-Parameters

Clicking the Generate button in the S-Parameter Generation dialog box (Analyze – [S] Generation) will generate the S-Parameters, as one would expect. These S-Parameters are derived in a manner similar to those employed by a Vector Network Analyzer (VNA), and as such can be considered “single-ended” S-Parameters.

When looking at differential pairs, it is often desirable to generate differential or mixed-mode S-Parameters. Both of these options are available, using the ts2dml"command. Typing this at your operating system command prompt will display the options available to convert single-ended S-Parameters to either differential or mixed-mode format.