



Development of a Design & Manufacturing  
Environment for Reliable and Cost-  
Effective  
PCB Embedding Technology

**AT&S**

**cādence<sup>®</sup>**

**THALES**



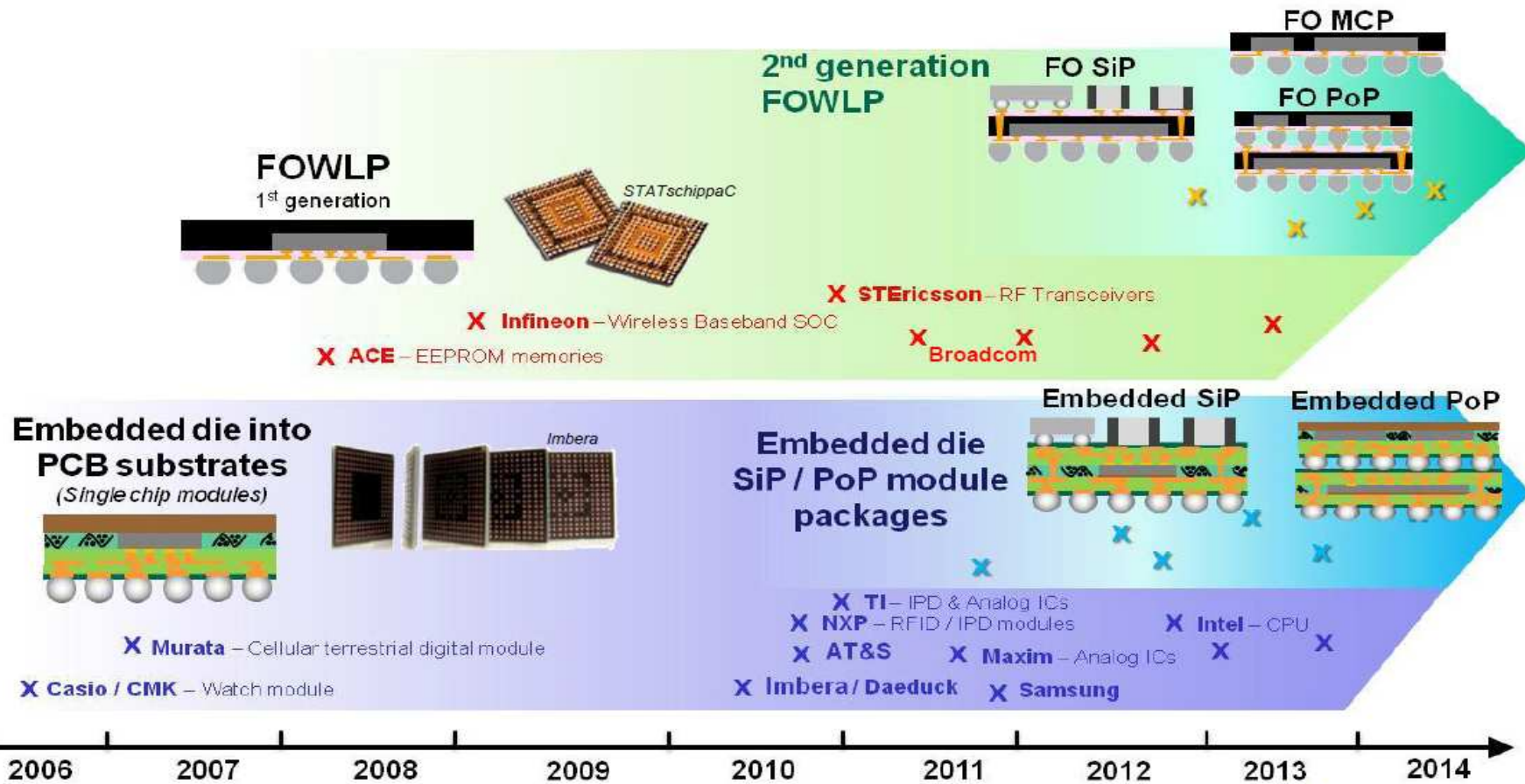
# Outline

- Introduction
- CAD design tools for embedded components
- Thermo mechanical design rules
- The industrialisation of chip embedding
- Conclusions and perspectives



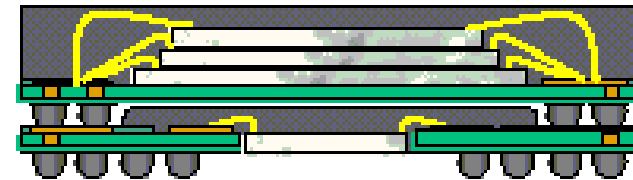
# The development of the chip embedding technology

## Embedded Wafer-Level-Packages Status of commercialization



# Miniaturization approaches

- Technology drivers that create large pin count devices
  - SoC – more functional density
  - SiP – mixed technologies with memory
- Miniaturization approaches used on PCB systems
  - Mezzanine boards
  - Rigid Flex circuits
  - High Density Interconnect
    - Shrinking pin pitch (< 0.8mm)
    - Large pin count devices
  - Embedded Passives
  - Low pin Actives



# PCB / IC-Packaging design tools requirements

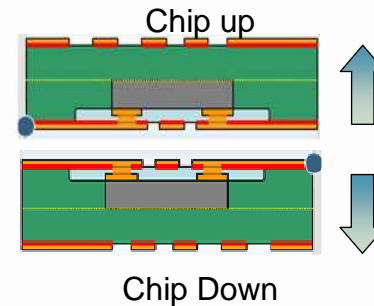
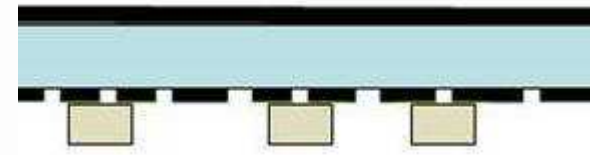
## Component, layer stack selections

Engineers specify

- Components to be embedded
  - “Embed Required” (Hard) or “Embed Optional” (Soft)
  - Ensures only qualified components get embedded
- Layers to be used

Style for embedding

- Chip-up, Chip-down
- Direct / Indirect attach



ID	Layer Name	Type	Thickness	Embedded Status	Attach Method
1	SURFACE		0.00		
2	TOP	CONDUCTOR	1.20	Not Embedded	
3		DIELECTRIC	8.00		
4	SIG_1	CONDUCTOR	1.20	Not Embedded	
5		DIELECTRIC	8.00		
6	SIG_2	CONDUCTOR	1.20	Not Embedded	
7		DIELECTRIC	8.00		
8	SIG_3	CONDUCTOR	1.20	Not Embedded	
9		DIELECTRIC	8.00		
10	SIG_4	CONDUCTOR	1.20	Not Embedded	
11		DIELECTRIC	8.00		
12	SIG_5	CONDUCTOR	1.20	Not Embedded	
13		DIELECTRIC	20.00		
14	SIG_6	CONDUCTOR	1.20	Chip Up	Direct Attach
15		DIELECTRIC	8.00		
16	SIG_7	CONDUCTOR	1.20	Not Embedded	

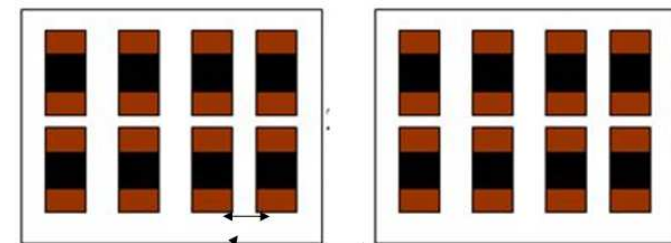
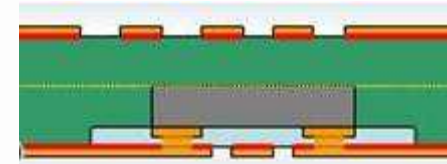
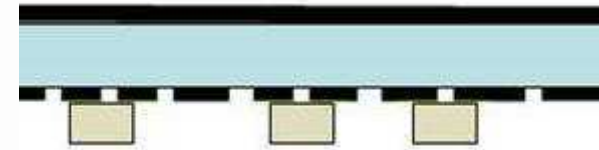
Embedded Global Parameters			
1. Cavity to etch layer clearance:	3.00	?	
2. Minimum cavity gap for merging:	20.00	?	
3. Placebound to via keepout expansion:	0.00	?	



# PCB / IC-Packaging design tools requirements

## Design Rule Checks

- Component to Component / Cavity
- Height checks – gap between component in cavity to adjacent metal layer
- Max cavity area
- Max number of components in cavity
- Vias within cavity area
- Metal to cavity area
- Extended cavity support based on component height



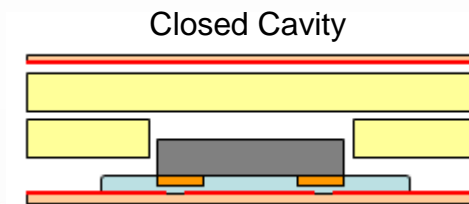
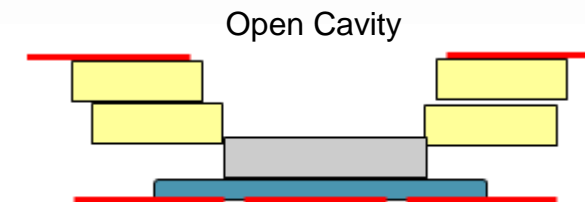
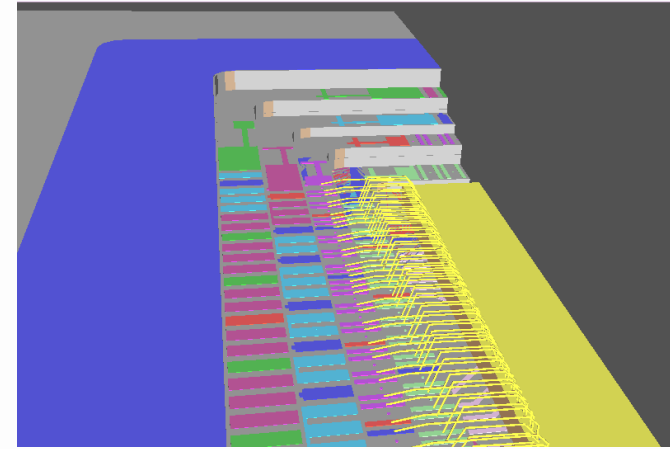
Comp to comp spacing

Cavity to cavity spacing

# PCB / IC-Packaging design tools requirements

## Cavity Support

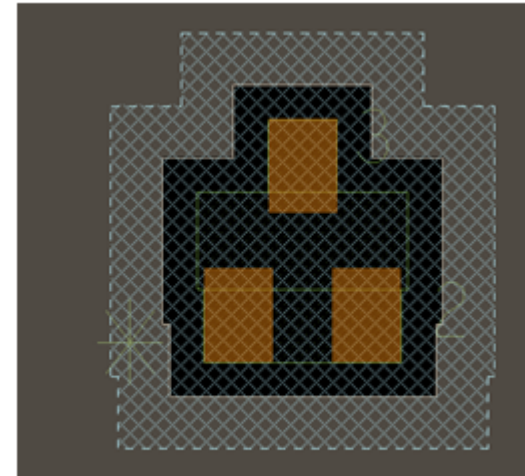
- Package driven
  - Keep-out properties
- User Defined Cavities
  - Manually created
  - Span multiple layers
  - Merge capability
  - DRCs
    - Max cavity area
    - Max comps within cavity



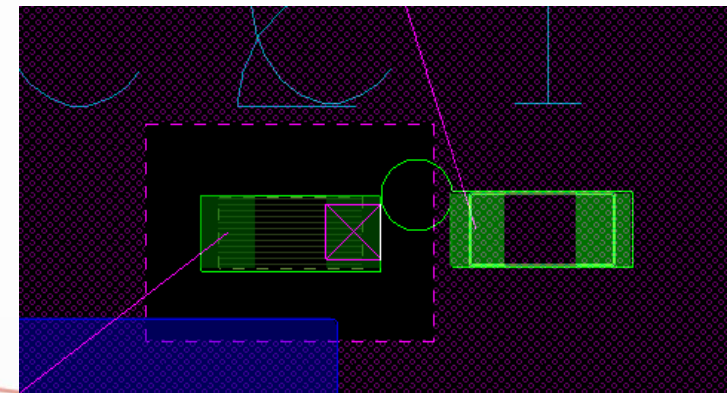
# PCB / IC-Packaging design tools requirements

## Constraint-Driven Place & Route, Mfg outputs

- Constraint driven place and route
  - Move components to inner layers
    - Don't put a via through the component!
  - Route to embedded components adhering to electrical, physical and manufacturing constraints
- Manufacturing outputs for layers with embedded devices
  - ODB++



Expanded Route Keepout area on protruding layer(s)

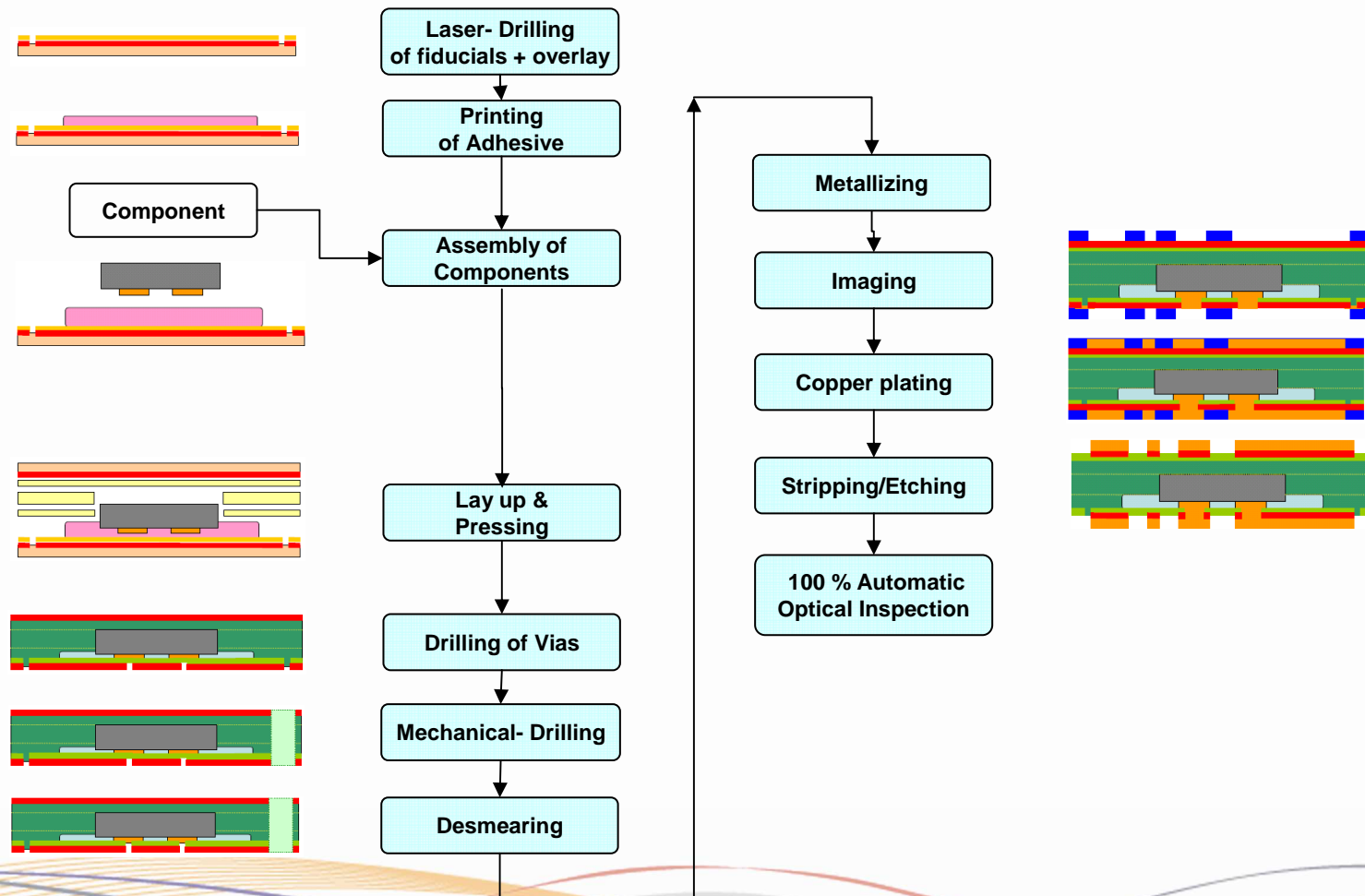


Dynamic Design for Assembly guided placement

# Checklist for EDA ECP capability

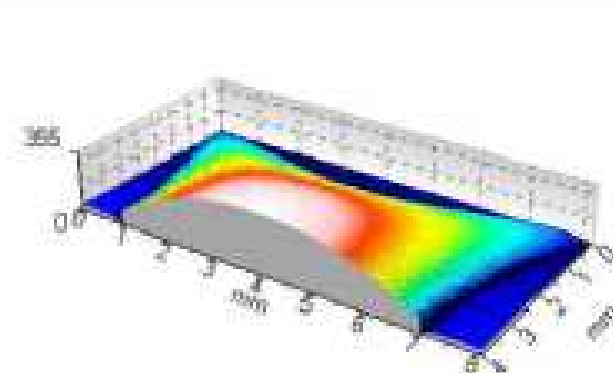
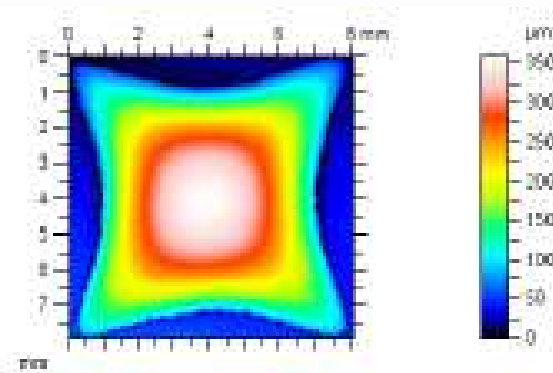
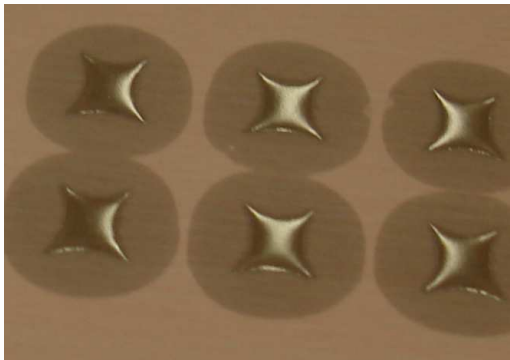
Supported	Planned	Workaround	Cadence
			Version: Allegro Beta 16.4
			HERMES Support Partner: THALES
			<b>Release: Planed Q2, 2011</b>
<b>Functionality for ECP®</b>			
			ECP® component placement between copper layers
			ECP® component pads available for via interconnect
			ECP® component with pads on top and bottom side
			Possibility to flip and/or rotate each ECP® component separately
			Component span over several copper layers
			Additional layers for ECP®- assembly, glue spots, cavities
			Separate assembly output for ECP® components
			ODB++ support for ECP®
			Gerber/Excellon support for ECP®
			Via-in-pad technology
			Filled/stacked via support for sequential buildup

# Process flow embedded core



# Adhesive printing

- Control of
  - feature size, shape and volume
  - By novel 3D scanner for large panels

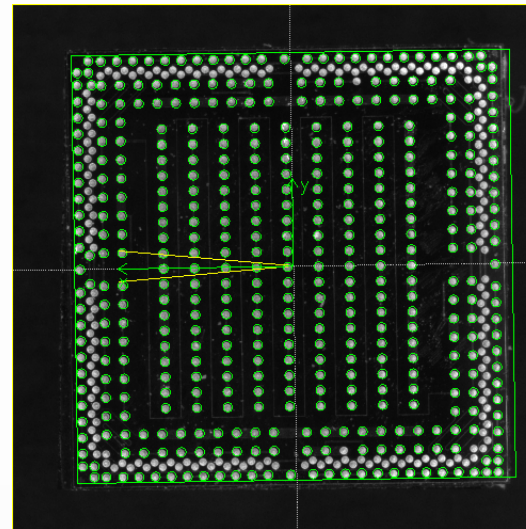


- determines the thickness and uniformity of the dielectric



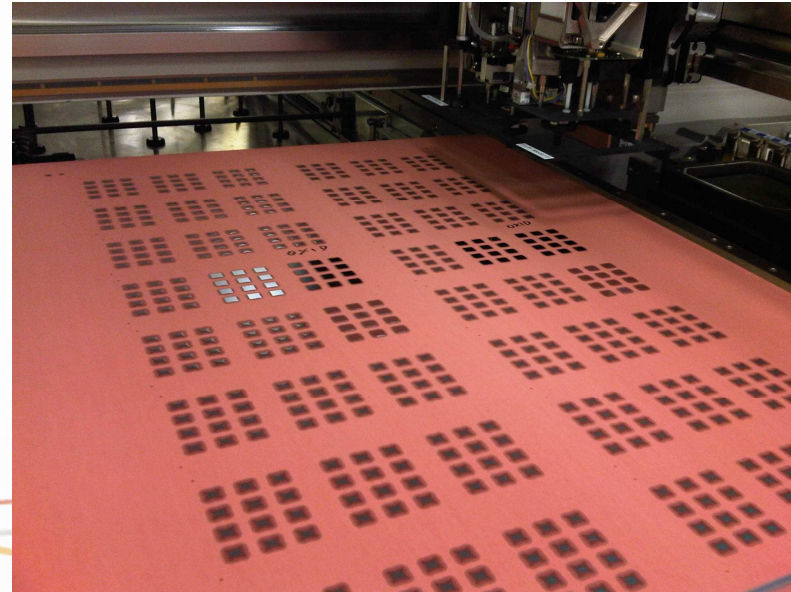
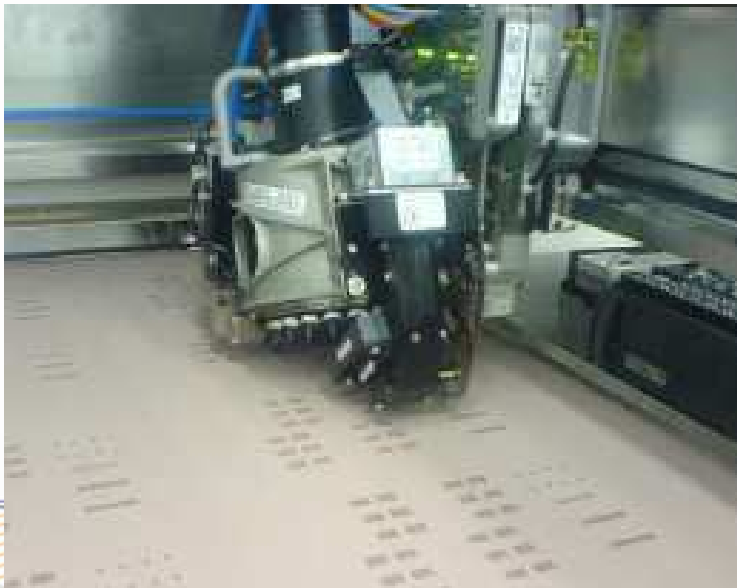
# Component Assembly

- Optical alignment of Flip Chip component
  - Requires high resolution cameras
  - Pattern recognition of pad design
- Design
  - Pad diameter: 150  $\mu\text{m}$
  - Minimum pitch : 200  $\mu\text{m}$
  - Chip size : 7 x 7 mm



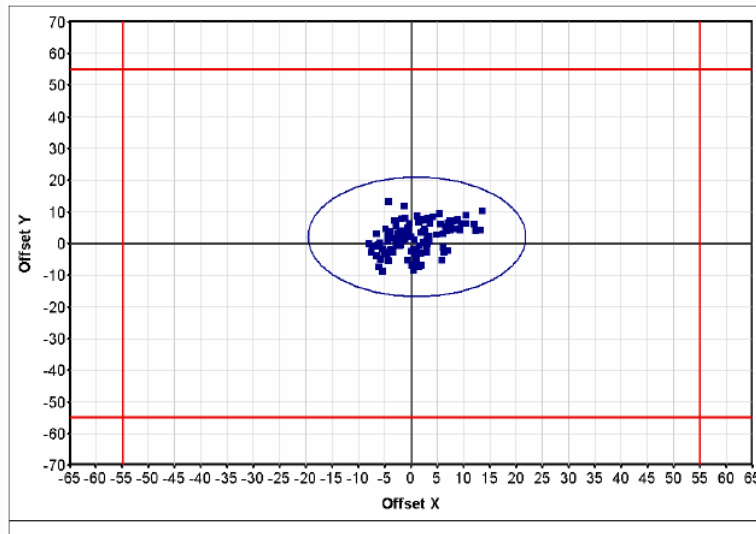
# Component Assembly

- Siemens X2 machine has two assembly heads
  - 20 nozzle head
  - For high through put
  - twin head
  - for high accuracy

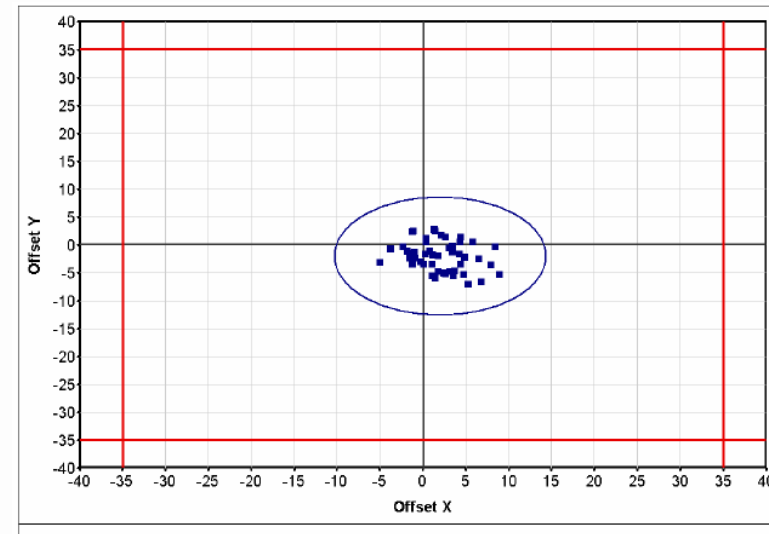


# Component Assembly

- Component placement accuracy
  - 20 Nozzle head
  - twin head



■ Resultfile: 2010-05-19\_14-22-17. (Value: Offset Phi, ItemType 0, Group: All, Angle: All\*)



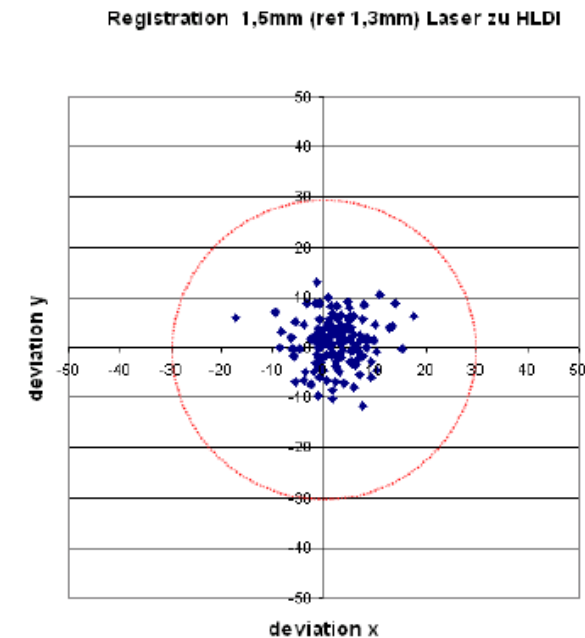
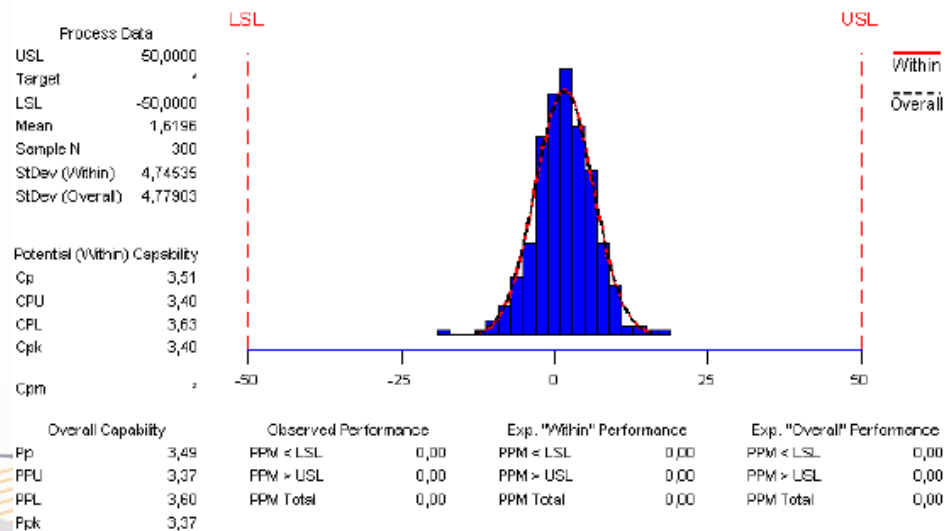
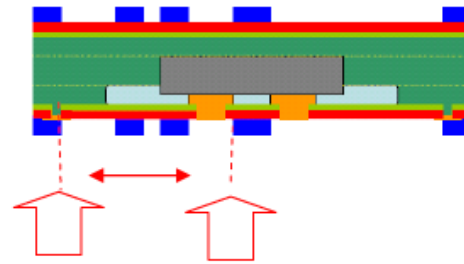
■ Resultfile: 2010-05-19\_18-07-51. (Value: Offset Phi, ItemType 0, Group: All, Angle: All\*)

	20 Nozzle head	Twin head
Max. speed	20000 comp/h	3700 comp/h
Accuracy specified	+/- 55 $\mu\text{m}$ , +/- 0,7°	+/- 30 $\mu\text{m}$ , +/- 0,07°
<b>Accuracy measured</b>	<b>+/- 20 <math>\mu\text{m}</math>, +/- 0,035°</b>	<b>+/- 11 <math>\mu\text{m}</math>, +/- 0,025°</b>



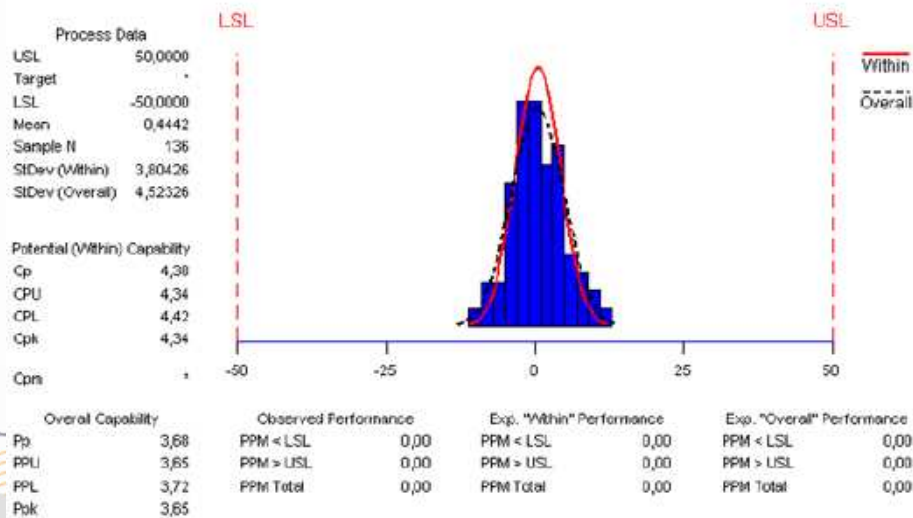
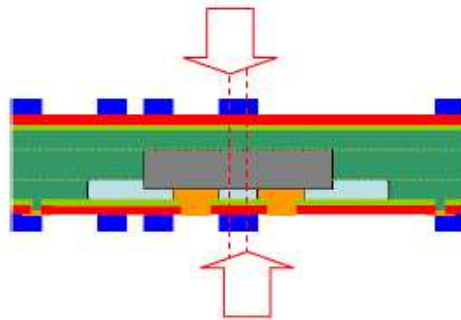
# 25 $\mu\text{m}$ technology

- Exposure with LDI – registration fiducial to pattern

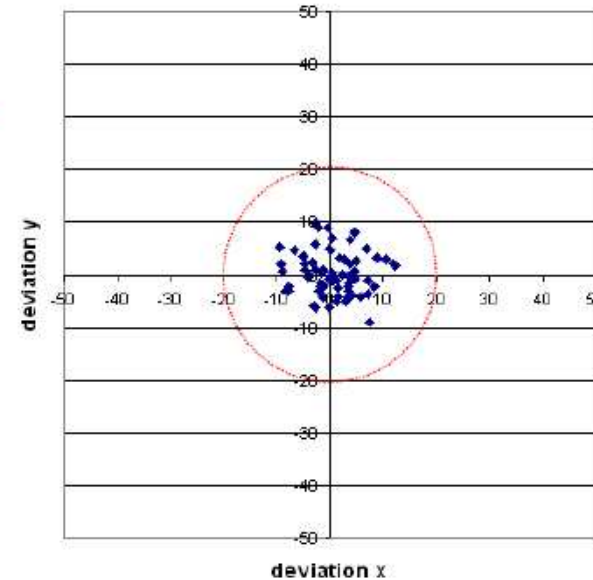


# 25 μm technology

- Exposure with LDI – registration front to back

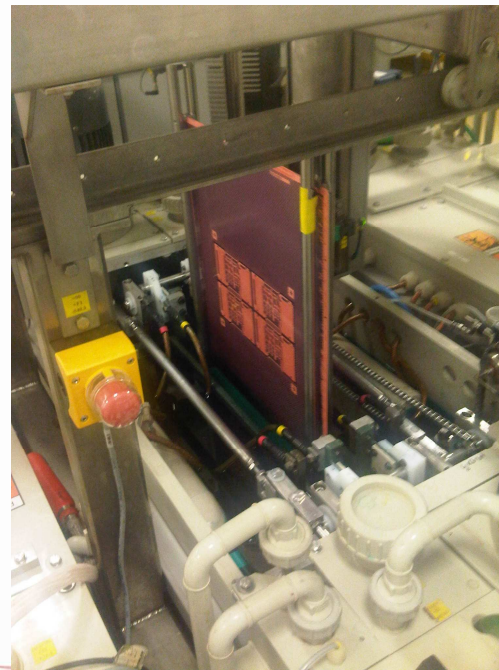


Registration accuracy Front to Back Paragon Ultra



# 25 $\mu\text{m}$ technology

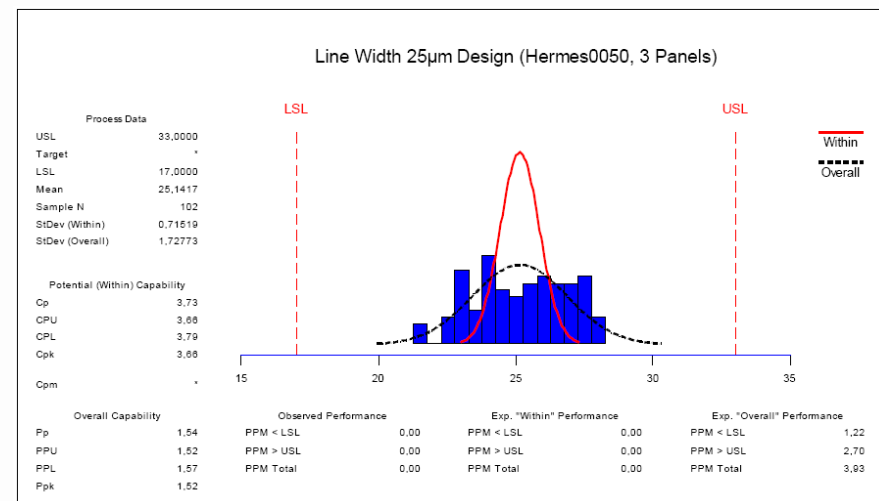
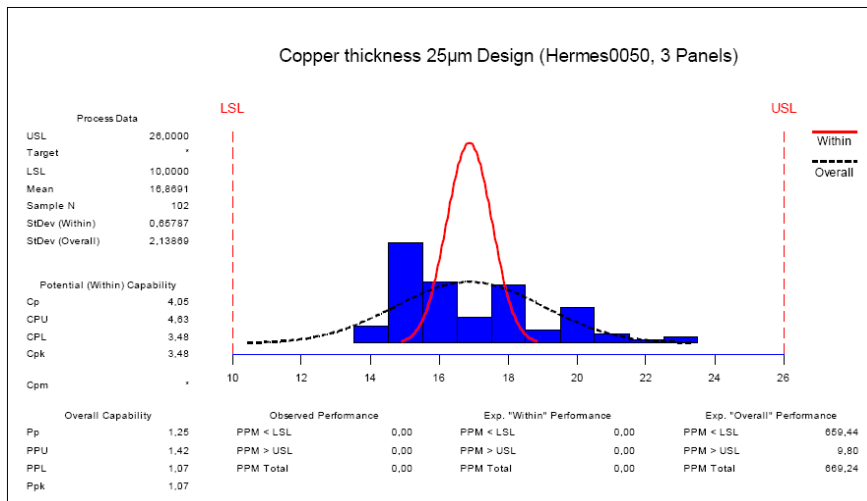
- Semi-additive technology – single board plater
  - Individual control of parameters of each panel
  - Handling of thin cores
  - Unique flow system
  - Pulse plating for via filling
  - Full traceability of process data
  - Single piece flow for improved
    - Flexibility
    - Risk management



# 25 $\mu\text{m}$ technology

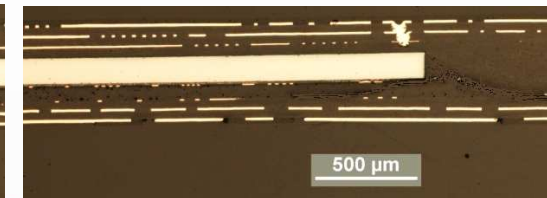
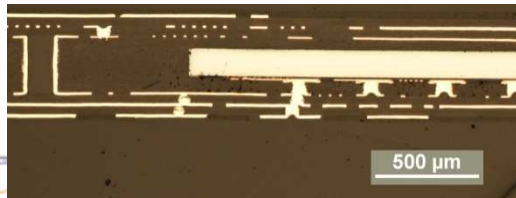
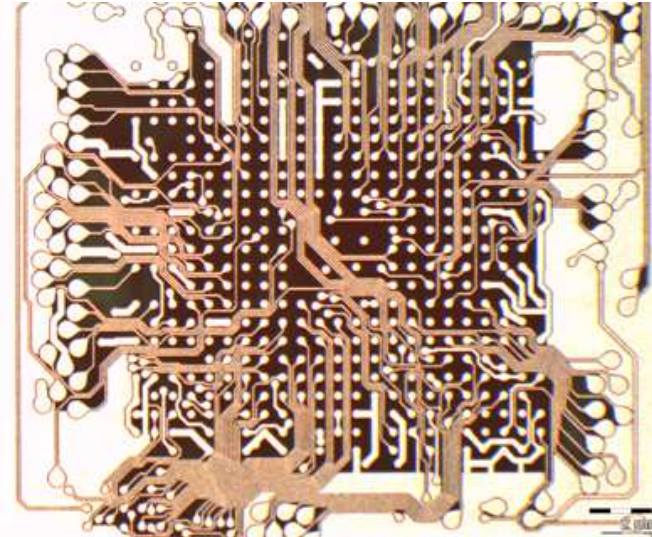
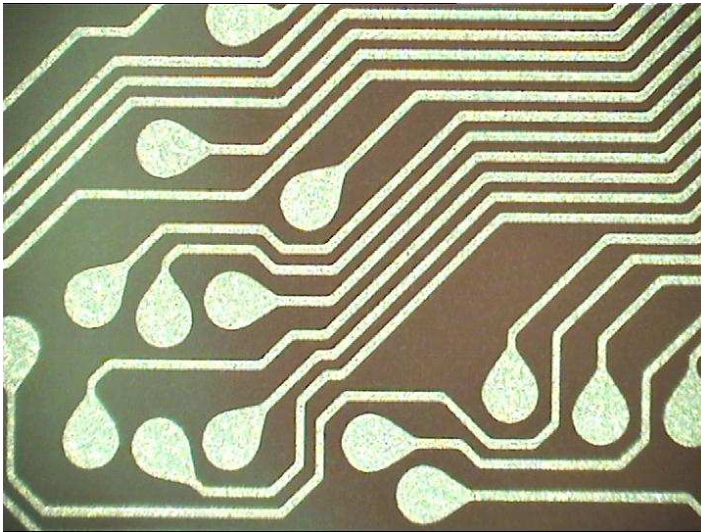
- Copper thickness

final line width



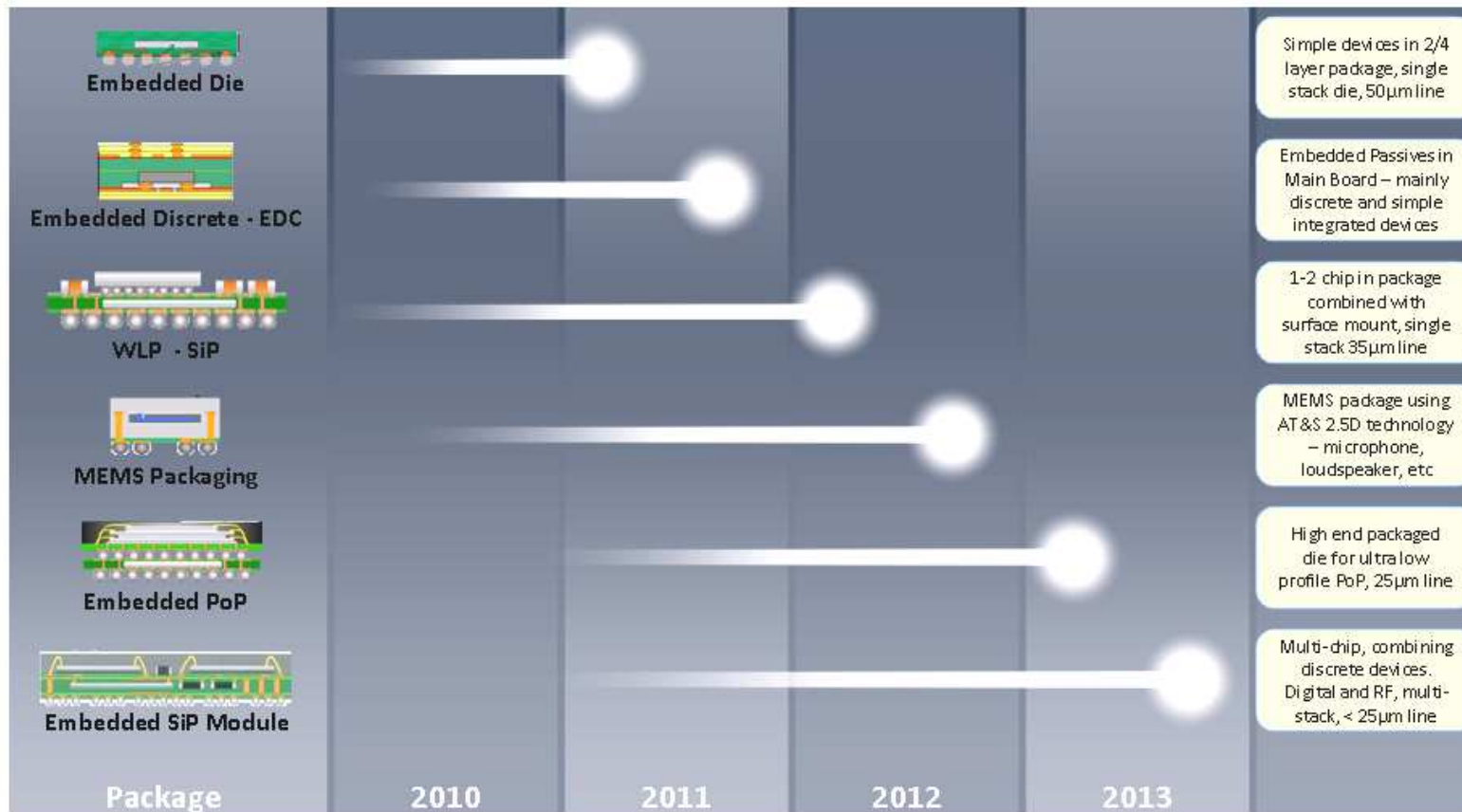
# 25 $\mu\text{m}$ technology

- Design of motor management module



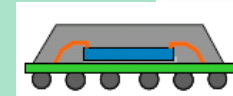
# Outlook for embedded modules

- Industrialization road map

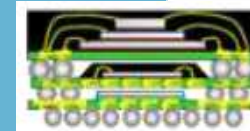


# Embedding Business

**GLOBAL IC Packaging market**  
**~ 270 Bunits by 2013**



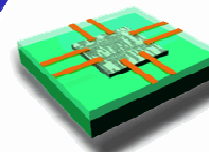
**TAM for «Embedding Ready» Components**  
**~ 20 Bunits by 2013**



**TAM** = Total Available Market  
for Embedded Components

**SAM** = Served Available Market

**SAM for Embedded Components**  
**~ 3 Bunits**  
**by 2013**



# Thanks for your attention

For more information, consult Hermes website

:

<http://www.hermes-ect.net>

