Full-chip electro-thermal simulation

using loosely coupled electrical and thermal simulators

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Session: 9.9
Drivers for 3D dynamic ETH sims

- Application profiles require higher temperature
- Temperature head-room reduces
  (operating closer to max. temperatures)
  - Thermal SOA (energy capability)
  - Bondwire / package reliability
- Power density goes up with improvement in performance of the technology
- Higher integration levels place power components on-chip closer to sensitive analogue circuitry
Temperature headroom reduces

- **Package reliability**
  - Molding compound degrades above a critical temperature:
  - Accelerated degradation of wire-bonds:

![Diagram of molding compound and wire-bonds degradation](image.png)

**Normal (fresh) molding compound**

**Decomposed after 225°C bake**
Temperature headroom reduces

Transistor Reliability

- Energy capability of power drivers
  - Self-heating + activation of parasitic BJT
  - Destructive!

Bias-temperature instability

- VT shifts over time at high temperature
- Both for LV as HV MOST’s
AMIS usage of the tool

Layout optimization for lowest TRise

- Tj,max = 230degC
- Tj,max = 209degC
- Tj,max = 185degC

Positioning of blocks
ETH simulation tool specs

- Annotate temperature at instance level
- Automatic capturing of power dissipation from instances
- Dynamic thermal response
- Including electro-thermal feedback loops (power dissipation depends on the hotspot temperature)
- Time-span of interest for the dynamic simulations
- Impact of package, bondwires on temperature distributions
- Evaluate alternative process options (thick metals)
- Fast enough to simulate complete functional blocks
Architecture of the Gradient solutions

Static tool flow

- Package Model, Bond wires, Ambient conditions
- Thermal Techfile (mask layer thickness, thermal parameters)
- Layout Database (post LVS, DEF/LEF GDSII, OA)

Tcl command File
(flow and control parameters, techfile options, power src details)

CircuitFire by Gradient Design Automation

Powersource b-boxes (derived/user-defined)

Optional TvsP Tables

Spectre (with device models and User control file)

Netlist annotated with instance temperatures

Instance power dissipation

Control commands

Instance temperatures
Architecture of the Gradient solutions

Static tool analysis modes

- Analysis modes support early stage design evaluation and detailed thermal analysis through:
  - Text based input for pre- and partial layout analysis
  - Full chip layout database for detailed, accurate analysis
  - Package interface compatible with $\theta_{JA}$ and ambient conditions
  - Control parameters for runtime/accuracy tradeoff
  - Instance specific and wire shape temperatures for annotation to electrical analysis tools; Full 3D visual GUI analysis

- Goal: Detect and avoid thermal hazards and reliability failures early in the design flow!!
**Architecture of the Gradient solutions**

***Dynamic tool***

1. **Package Model, Bond wires, Ambient conditions**
2. **Thermal Techfile** (mask layer thickness, thermal parameters)
3. **Layout Database** (post LVS, DEF/LEF GDSII, OA)
4. **Power Source Waveforms**
5. **Tcl command File** (flow and control parameters, techfile options, power src details)
6. **Optional TvsP Tables**
7. **HeatWave by Gradient Design Automation**
8. **Powersource b-boxes** (derived/user-defined)
9. **OA Design database**
10. **Spectre** (with device models and User control file)
11. **Control commands**
12. **Instance temperatures at simulation time intervals**
13. **Netlist annotated with instance temperatures**

- HeatWave by Gradient Design Automation
- Spectre (with device models and User control file)
- Control commands
- Instance temperatures at simulation time intervals
- Netlist annotated with instance temperatures

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Architecture of the Gradient solutions

**Dynamic tool analysis modes**

- Thermal hazard analysis due to transient temperature propagation during floorplan and post-layout stages with
  - Synchronized thermal simulation with user’s electrical simulator
  - Adaptive time step control based on thermal parameters
  - Monitoring of min/max instance temperatures and temperature differences between instances as a function of time
  - Automatic reporting of temperature violations
  - User defined control parameters for speed vs. accuracy
  - Uses same design database as steady state
  - Interface with transient package models in progress
  - Visual GUI with pause and playback features for insight into transient thermal effects
Architecture of the Gradient solutions

- Dynamic analysis: surface plots & waveform

![Graphical representation of dynamic analysis with surface plots and waveform data for Two Transistor Power Sources.](image)
Architecture of the Gradient solutions
Benefit of the loosely coupled scheme

- Allows interface between HeatWave and existing electrical simulators
  - Allows fast feedback of electrical power values

- Provides significant performance improvement
  - Thermal network node count is orders of magnitude larger than electrical network
  - Low overhead of thermal simulator allows fast temperature updates to electrical simulation models
  - Compared with direct coupled simulation orders of magnitude speed-up!!

- Thermal simulation control parameters allow for speed-accuracy trade-off independent of electrical simulator
Conclusion & future work

Conclusions

- We implemented a full-chip electro-thermal simulation flow
- Loose coupling between the electrical and the thermal simulators provides a more advantageous speed trade-off

Future work:

- Package thermal model
  (transient successor to Delphi models)
- Incorporation SIP / APD flows (?)
CONNECT: IDEAS

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