Model-based Verification and Analysis for 65/45nm Physical Design

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ABSTRACT

For 90nm technologies and above, manufacturability analysis and sign-off was mostly limited to required and recommended Design Rule Checks (DRC).
Developed for 45nm and under test for 65nm, we see a new methodology emerging: more complex manufacturability rule decks (MRD) are used to classify potential circuit or geometric violations ("hotspots"). Then scoring rules are applied to predict overall manufacturability, and prioritize hotspots for manufacturability improvement. Rule-based checking is enhanced with physical simulators, for simulation of random yield loss and of systematic effects, including Lithography and CMP.
IBM and Cadence are developing a software infrastructure that combines MRD checking and yield simulation. This software allows for integration of different (including 3rd party) simulators, and also for coupling of different physical effects. The software's output can be used for sign-off purposes, process optimization or can be input to electrically-aware layout optimization tools. It can increase yield and reduce turn-around-time by optimizing design and process windows.
In this paper, we will present more details on a first version of this architecture and analysis flows that combine MRD checking with random yield analysis. These flows include software for automatic scoring of manufacturability hotspots and can generate input for automatic library and full-chip optimization.

1 Introduction

A Design Rule Checking (DRC) deck typically consists of several hundred rules that can be executed by *DRC tools*. Rules are composed of basic operations on a geometry database. These operations include geometry manipulations and connectivity checks. Each rule typically represents a limited yield loss mechanism. For example, some yield loss due to lithography issues is represented by width-and-spacing rules or yield loss due to CMP effects is represented by density rules, etc.

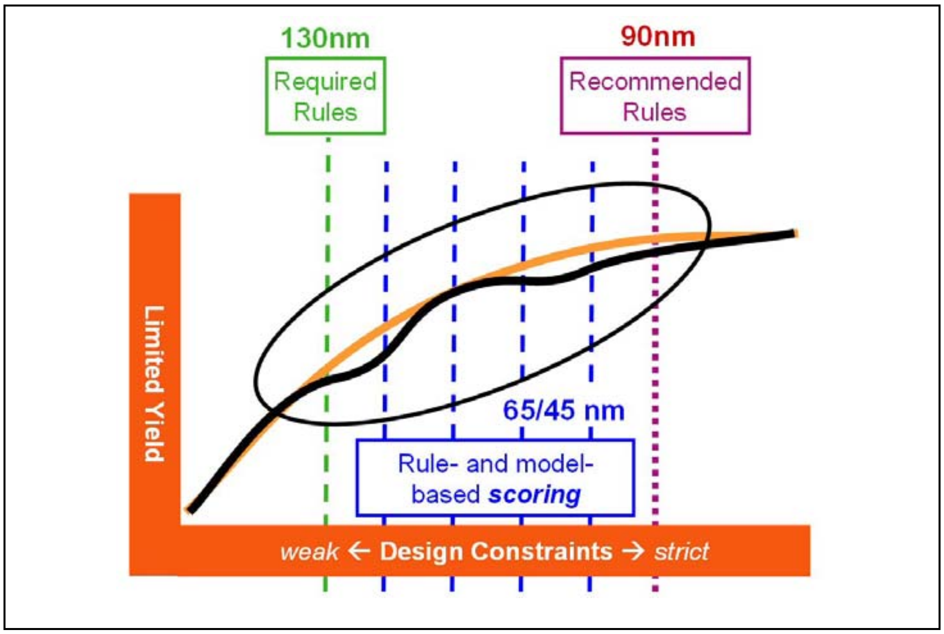


Figure 1: Evolution of the DRC concept from 130nm and older technology nodes to 65 and 45nm. Original single restricted rule decks were extended with recommended rules, to now also include prioritization and scoring.

Figure 1 shows how rule-checking methodologies have evolved since 130nm and older technology nodes. At 130nm, the manufacturer provided a single rule deck to the designer. Each rule was calibrated such that, when passed, a given limited yield for the underlying physical effect could be expected. For 90nm, *recommended rule decks* were provided, in addition to the single *restricted rule decks* provided at 130nm. A design has to pass all restricted checks before it can be manufactured. If it also passes the recommended rules, the manufacturer expects higher yield, and manufacturing services can be offered at a better price point.

For 65 and 45nm, manufacturers are now experimenting with rule decks that do not only provide pass/fail criteria, but that classify rule violations according to priority [1]. Typically, four to six such priorities are defined and implemented in the same language as a restricted or recommended DRC deck. We will refer to these new decks as Manufacturability Rule Decks.

Design and manufacturability rule checking can be performed at reasonable execution time. However, yield simulation accuracy is limited, and complicated physical effects are impossible to model. Even though the typical MRD includes checks for most random and systematic yield loss mechanisms, separate sign-off flows are being developed to perform more accurate, albeit more compute-intensive checks for the most important random and systematic yield loss mechanisms. Such flows include simulations of defect-limited yield loss, via failures, and lithography and CMP-related manufacturing problems. Since, typically, these new, isolated flows operate with different technology and geometry databases, coupling of the different physical mechanisms cannot be modeled. For example, CMP-related dishing may cause a device failure due to lithography de-focus: this can not be modeled with independent CMP and lithography simulations.

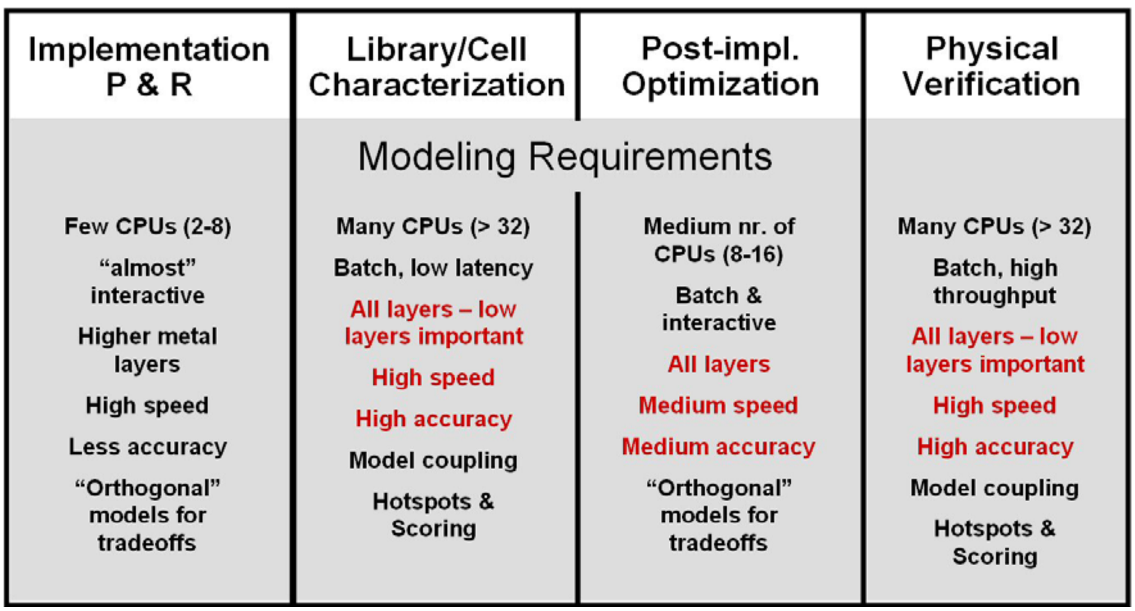


Figure 2: Changing modeling accuracy vs. performance trade-offs for different parts of the design flow.

In general, the physical simulation of different yield loss mechanisms can be performed at different accuracy levels and execution times. For instance, for the simulation of defect-limited yield, critical area can be calculated exactly, at high computational complexity, or by sampling the underlying layout, a commonly employed method that drastically improves run times but sacrifices resultant accuracy.

Figure 2 shows how modeling requirements change as the designer moves from back-end-of-line (BEOL) and front-end-of-line (FEOL) implementation—in library development and wiring interconnect—to design tape-out (requiring post-tapeout verification and optimization, such as optical proximity correction (OPC) or resolution-enhancement techniques (RET). Depending on the available compute power, required turn-around times, and necessary modeling accuracy, the accuracy/compute requirements of physical modeling at different stages of the design change. Since sign-off tools such as DRC software is used at all stages of the flow, these varying requirements have to be accounted for in new sign-off methodologies, including physical modeling. Because of these different requirements, depending on position in the design flow, yield physics are either modeled rigorously, or represented by compact and empirical models, or by geometric rules, much like in older DRC decks.

Under the project name Project-Dependent EDA (PD-EDA), since May 2007, IBM and Cadence have been developing a software infrastructure combining MRD checking and yield simulation. This software allows for integration of different (including third-party) simulators, and also for coupling of different physical effects. To the user, the input to the software is very similar to what was previously used for manufacturability checking. PD-EDA assumes that an MCD is extended with operations that invoke yield simulations and operate on intermediate data of the *same* software flow. The software's output—namely hotspots, yield predictions and scores—can be used for sign-off purposes, process optimization or can be input to electrically-aware layout optimization tools.

After this introduction, we will describe PD-EDA in more detail, including motivation and goals, software architecture and application flows. Then we will provide more details on an important component of PD-EDA, namely the software used to perform defect-limited yield analysis via critical area calculation.

2 PD-EDA

For 65 and 45nm, we see MCD flows evolving in parallel with the following sign-off and optimization flows, among others:

- Timing and performance.
- Random yield analysis (see, for instance [2]) and optimization (via optimization, wire spreading and widening).
- Litho Process Check (LPC) [3]: after application of "trial OPC", the lithography process is simulated and layout contours are generated. Then design rule checks are performed on generated contours, to find "Litho hotspots".
- CMP simulation and intelligent fill [4]; fill patterns are generated after CMP simulation, to reduce the impact of potential failures such as dishing, pooling, etc.
- Some manufacturers are storing libraries of patterns which are known to cause yield problems. Before manufacturing a design, a new layout is analyzed and some design patterns are substituted with geometries that are easier to manufacture, based on past experience.

Even though these flows use/generate conceptually similar input/output data, they run in isolation, i.e., require separate geometry databases, technology information, user interfaces, and sometimes also different types of compute resources.

Two of the major goals of PD-EDA are the elimination of overlaps between the different sign-off and optimization flows, and the integration of different modeling and MRD checking capabilities to allow for coherent hotspot scoring. For example, a global prioritization mechanism is used to prioritize some litho hotspots over other random-yield hotspots.

The integration also permits correlations between different physical effects. A single hotspot output interface is used to generate input to several optimization tools: to address requirements for standard cell libraries vs. large digital chips, for instance. This will permit different optimization techniques for FEOL and BEOL.

2.1 Architecture

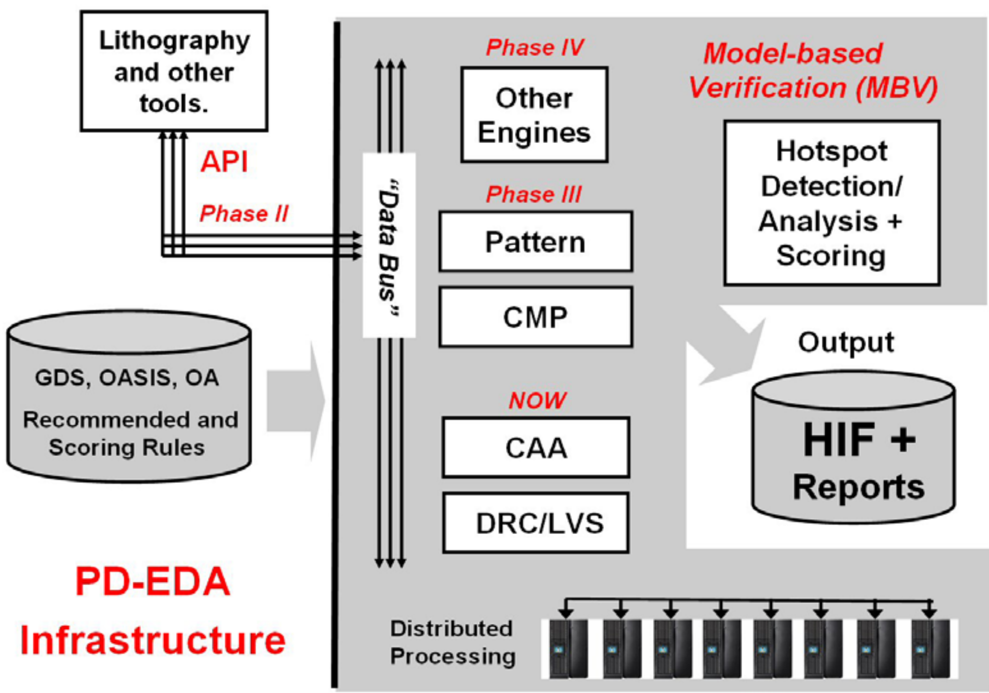


Figure 3: Architecture of PD-EDA's software infrastructure including MBV, a tool for Model-Based Verification.

Figure 3 depicts the software architecture of the infrastructure that we are developing. As input, the Model-Based Verification (MBV) tool, developed at the core of the PD-EDA infrastructure, accepts a layout database in GDS, Oasis or OpenAccess format. As output it generates, among others, hotspots in Cadence's open-standard Hotspot Interface Format (HIF) [5]. Similar to a DRC violation, a hotspot consists of a geometric marker, an edge, vertex or polygon that identifies a location on a design layer prone to manufacturability problems. In addition to the geometric location, each hotspot in HIF is stored together with *hints* for possible optimization.

With MBV, an underlying geometry processing engine that can handle DRC and LVS operations is first extended with Critical Area Analysis (CAA). For CAA, we are using a software library ("Voronoi") developed and used in production by IBM [6]. We will provide more technical details on Voronoi in Section 3. In the project's second phase, we are providing an external API for the integration of external, geometry-based checking tools, such as lithography simulators. Third, we are planning to integrate CMP simulation and pattern detection and usage. Depending on the requirements for 32nm, we will flexibly enhance the system by adding additional capabilities, as, for instance, etch simulation. The entire system can be used on an underlying distributed parallel compute platform.

The base DRC engine operates on geometries and layers, stored in memory. Temporary data are stored in similar data structures. Fast access to these data by the other infrastructure components enables model coupling of different physical effects, such as lithography and CMP, or to calculate critical area on nets selected by previous DRC operations. Also the overall system operates on a single layout database, and hotspots are scored, as part of MBV, in a single software module assessing and comparing manufacturability problems for different yield-loss mechanisms.

2.2 Application Flows

We are developing three usage flows in PD-EDA.

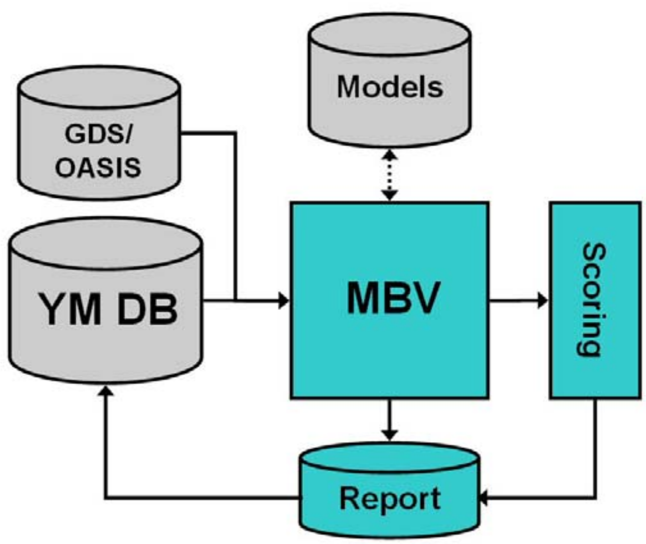


Figure 4: PD-EDA Manufacturing Flow.

Figure 4 depicts the "Manufacturing Flow". MBV is used as a closed system for random-defect yield analysis. I.e., process characterization data such as failure rates are read from a DB2-based Yield Management system and combined with layout attributes extracted from a layout to predict limited yield loss for several failure mechanisms. Via failures are simulated via multiple models; defect limited yield is modeled via CAA; and random device failures are modeled by geometry extraction of transistors and devices of specific shape, perimeter, area or other characteristics. This first flow is used as sign-off system by both process and design engineers. In addition, on the process side it can be used for process monitoring, characterization and optimization.

A second flow, the “Library/Macro Flow” shown in Figure 5, is being developed for the characterization of standard-cell libraries and macros. To facilitate use, we start from a customized layout editor. Then, hotspots are generated in HIF format by MBV, based on MCD and physical simulations. The hotspots can be visualized in the editor, for manual fixing, or used by a subsequent optimization tool. In PD-EDA, optimization is performed by software proprietary to IBM, performing small layout modifications (edge and vertex movements) based on the solution of a large, non-linear system of constraints. Alternatively, we are considering the use of a compactor. By developing the Library/Macro flow, we will gain first experience in combining rule-based analysis with the most prominent failure mechanisms, such as random defects and lithography. This flow will be used by standard library and macro designers.

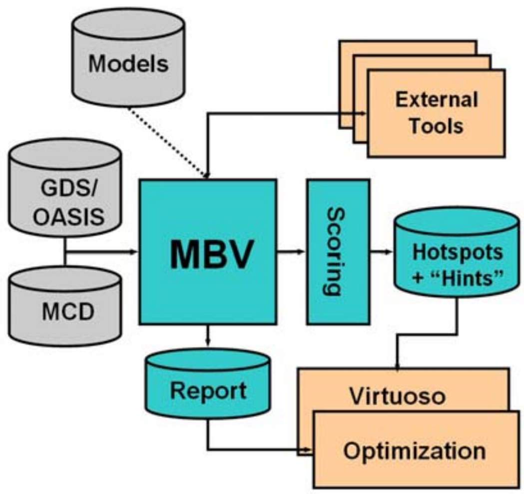


Figure 5: Library/Macro Flow.

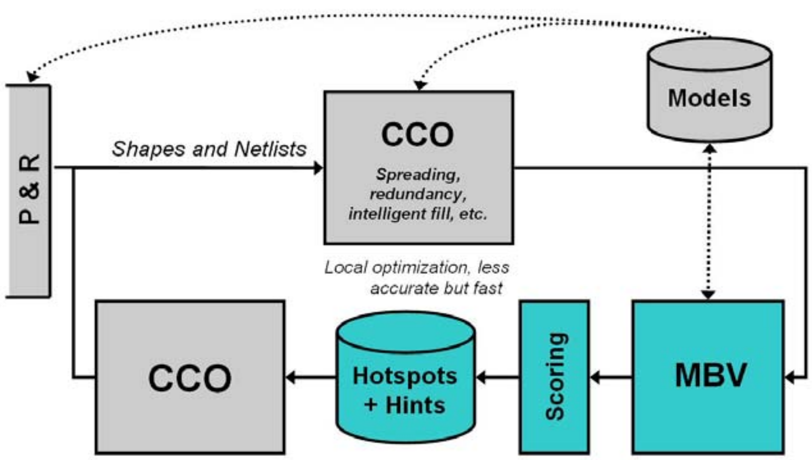


Figure 6: Digital Flow.

A third flow (Figure 6) is targeted towards sign-off and optimization of large digital designs. Cadence Chip Optimizer (CCO)[1] can be used to perform post-tapeout optimizations, such as via reduction and insertion, wire spreading and widening and intelligent dummy fill [7]. It is based on modeling methods that put high emphasis on execution performance. Also, typically, optimizations are not performed using the same prioritization method implemented in MCDs and required by the manufacturer. In this flow, we follow a CCO run by performing full MCD analysis with MBV, including simulations. Since MBV simulations are performed at highest accuracy, and manufacturer-approved scoring methodologies are applied, a clean MBV run implies sign-off of CCO's layout optimizations. If MBV detects hotspots, they are provided in HIF format to CCO to execute an additional optimization loop. The primary use of the third flow will be during and after place-and-route, after design integration and at sign-off time. In a previous study [8], it was shown that on a typical 45nm design, more than 85% of all MCD-based hotspots could be fixed.

2.3 Hotspots and Scoring

Rule Intent	Nr. Rules per Score/Priority					Density	Performance
	1	2	3	4	5		
OPC Correction	2		1	2			
Critical Area / Random Defects	8	2	5	2			
Device Control	2		1				
Contact Area		4	1				
Support Assumed Current	1	1	1				
Via Redundancy	6		5				
Via Overlap	8		6	1			
Mini. Impact of corner rounding		1					
Litho limitation				1	6	1	
CMP uniformity/prevent litho flare						3	
Placement of device end parallel to gate							7
Min. width for redundant contact							1
Limit CA density for stress enhancement							2

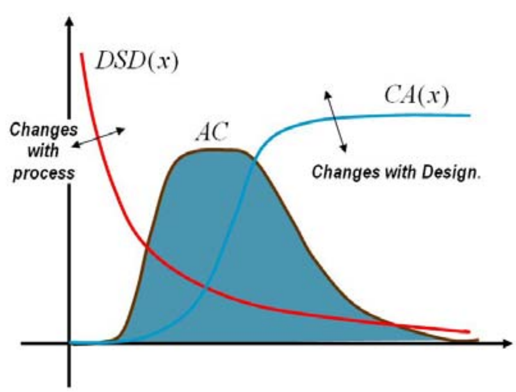
Table 1: Example 45nm MCD showing the number of rules for each priority class and physical rule intent.

[1] CCO is one result of another joint collaboration between IBM and Cadence, a project also referred to as MAR, Catena, or Finale.

Hotspots are generated for rules and simulations in HIF. Similar to the output of a DRC tool, they consist of geometric layout attributes such as layer, cell and instance, and either vertex, edge or polygon describing the location and shape of a hotspot. In addition to the normal DRC output, HIF includes hints for fixing hotspots. Typically these hints consist of either (1) suggestions for edge or shape movements, or (2) suggestions for replacing an entire geometric pattern with another one (i.e. several polygons), or (3) larger bounding boxes of layout segments that need to be re-routed with new, stricter constraints. Similar to an expert system, after reading and analyzing an HIF file, the scoring software evaluates prioritization rules. These rules are defined when the underlying process is developed (similar to DRC decks).

In Table 1, we have summarized the contents of a typical 45nm MCD. The limited yield-loss mechanism underlying each rule is listed along the y axis of the table. The x axis lists five priority buckets, and the table shows how many rules for each failure mechanism fall in each bucket. In this example, density and performance violations are handled outside of the scoring flow. Note that about half of the rules refer to FEOL and the other half to BEOL. BEOL violations can possibly be fixed with CCO; FEOL can be addressed at the cell level with editing or other optimization technology. Note also that the MCD includes rules for approximated CAA, litho and CMP checks. Therefore, added rigorous simulation of these yield-loss mechanisms would only add accuracy to functionality already covered in more primitive form by rules in the MCD.

3 Voronoi Critical Area Analysis



$$Y = e^{-\int_{x_0}^{x_{max}} DSD(x) \times CA(x) dx}$$

$$AC = \int_{x_0}^{x_{max}} DSD(x) \times CA(x) dx$$

Figure 7: Poisson Yield Model; *x* is the defect size, *DSD* the Defect Size Distribution, *CA* the Critical Area, *Y* the Yield and *AC* the *failure coefficient*, also sometimes called *thetabar*.

Figure 7 outlines the Poisson model for defect-limited yield [9]. The manufacturer provides failure rates for different defect sizes as a probability function, also denoted as Defect Size Distribution (*DSD*). Critical Area (*CA*) is the area on a given layer on which a defect of a given size can fall to create either electrical open or short. Because any layout consists of a discrete number of polygons, *CA(x)* is a piecewise linear function of *x*, the defect size. Given a minimal and maximal defect size, the integral AC of the product of DSD and CA (also called *failure coefficient* or *thetabar*) can be used to predict yield.

3.1 CAA Algorithms

In practice, three different algorithms are used to calculate critical area.

3.1.1 Dot Throwing

Simulated defects ("dots") are generated in the layout, and the effect of each dot (whether it causes a short or open) is tallied. This process is repeated a sufficient number of times to produce an acceptable estimate of critical area, using Monte Carlo error analysis.

3.1.2 Size-based

Using a combination of Boolean operations and DRC-type sizing operations, critical area polygons are computed and overall area is calculated. This algorithm requires one sizing and one Boolean operation for each defect size. Since maximum defect sizes are typically large, this algorithm is very compute intensive; sizing polygons in a hierarchical layout by large amounts essentially destroys the underlying layout hierarchy. Both Boolean and sizing operations are based on scan-line algorithms [10, 11]. Also, unless all defect sizes of the piecewise-linear CA function are included, the result of the size-based approach is by definition an approximation; interpolation must be used to extract the entire CA curve.

3.1.3 Voronoi

This method was developed at the IBM T.J. Watson Research Center [12] and is based on calculation of Voronoi diagrams for each design layer; these diagrams are a partitioning of the plane encoding nearest-neighbour information of the layout shapes on a layer. Constructing the Voronoi diagrams and calculating critical area can both be performed by use of a single scan-line algorithm. The critical area curve is computed completely, for all defect sizes. As part of PD-EDA, we have added capabilities to the original Voronoi library, including connectivity-based CAA, and sampling. Accounting for connectivity strongly increases CAA accuracy. For instance, when two shapes are "opened" by a defect, connectivity analysis will determine whether both shapes do not cause any open due to redundancy; cause a single open because the two shapes belong to the same net; or cause two opens because the two shapes belong to different nets. Among the three algorithms, Voronoi provides the *best performance at the highest accuracy*.

3.2 Results

This section shows two example results generated with MBV/Voronoi. Figure 8 depicts *AC* on a metal layer of an X-routed test design [13]. *AC* was calculated on a 512x512 grid for this example, by calculation of *CA(x)* for all defect sizes and each point of the grid. We are currently performing hotspot analysis using this grid-based approach, but we will extend the underlying software to also work at shape-level with higher resolution in the near future.

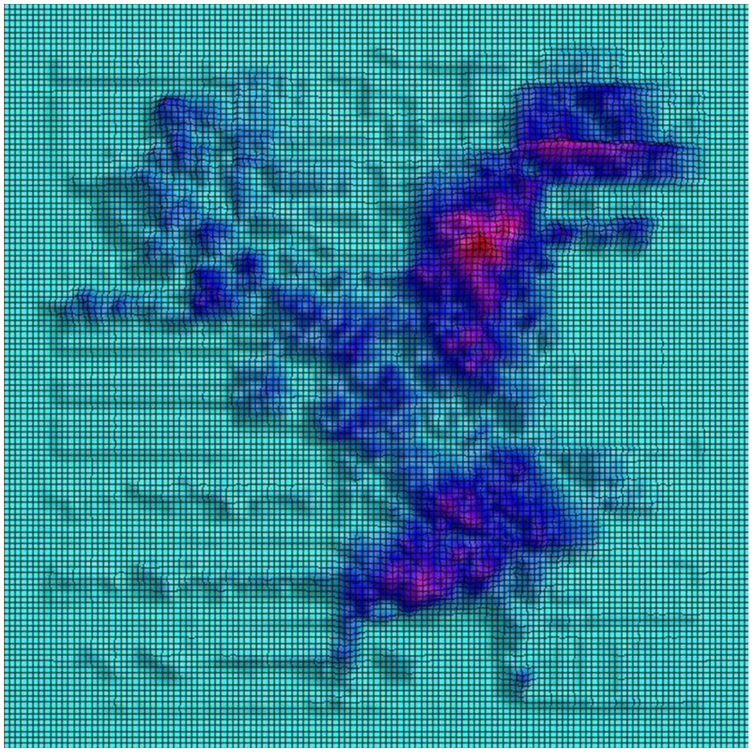


Figure 8: AC on an X-routed design.

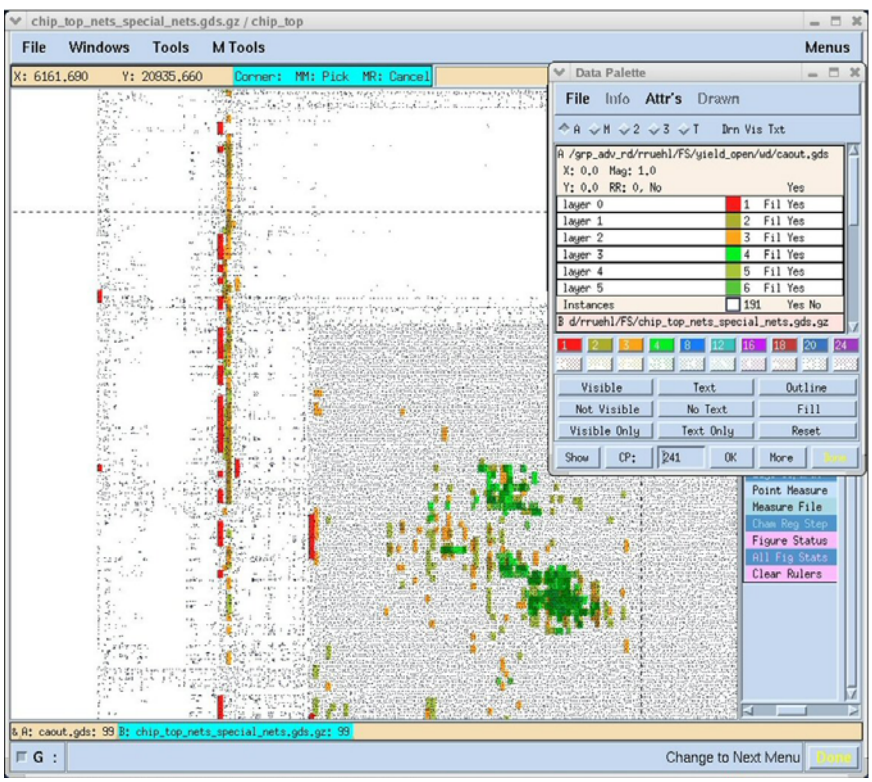


Figure 9: Yield hotspots for Opens and 6 metal layers, overlaid with instance map of original design in QuickView.

AC can be used to calculate critical area hotspots that can both be exported into HIF or in GDS/OASIS/OpenAccess. When in GDS/OASIS/OpenAccess, hotspots can be displayed in a layout viewer and overlaid with the original design. Figure 6 shows an example for Open failures on six metal layers displayed in QuickView [14].

Conclusions

For 45nm, a sign-off methodology is emerging that is also being applied to newer 65nm designs. Manufacturability checking decks replace Design Rule Checks, and additional physical simulators are employed for more accurate modeling of random and systematic yield loss mechanisms. The most prominent random loss mechanisms include random defect-limited, via and device yield. On the systematic side, first lithography and CMP are considered. Scoring is applied for overall manufacturability prediction and to prioritize hotspots for manual or automatic fixing.

As part of PD-EDA, we are developing a model-based sign-off infrastructure. This infrastructure combines MRD checking and physical yield simulation. In addition to integrating currently separate flows, it will greatly enhance sign-off efficiency. Also, it will allow coupling rule checks and physical simulations in a way previously not possible. Finally, a link to tools for automatic, electrically-aware layout optimization, for both FEOL and BEOL is under development.

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