DDR2 and DDR3 Challenges

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Session # 8.4
Outline

1. Comparing DDR2 and DDR3
   1. Tree Topology
   2. Fly-By Topology
   3. Data Channel

2. Using Allegro PCB SI
   1. Post-layout analysis using Bus Analysis in Allegro PCB SI
   2. Timing Budget for DDR2 and DDR3
   3. Comprehensive simulation in Allegro PCB SI
   4. S-Parameter Package Model in Allegro PCB SI

3. Correlation – Lab versus Simulation

4. Summary
Topology

- **DDR2 memory modules uses tree topology which**
  - Increases number of stubs and stub length
  - Signal arrival time is same on each DRAM
  - Address/Command/Control has a VTT termination on the system board
  - Less data–eye margin

- **DDR3 memory modules uses fly–by topology which**
  - Reduces number of stubs and stub length
  - Causes interconnect delay skew between clock and strobe at every DRAM on DIMM
  - Address/Command/Control has a VTT termination at the far end of the bus on the module
  - More bandwidth
Write Levelization

\[ t_{\text{Delay}} + t_{\text{DQSMB}} = t_{\text{CKMB}} + t_{\text{CKREG}} + t_{\text{CKDRAM}} \]
Tree Topology

DDR2

Controller
DDR2 UDIMM Clock Topology

- 60 ohm Trace

Controller > Connector > DRAM

200 Ohm
• DDR3 UDIMM nets have unloaded and loaded sections on Address/Command/Control topology
• This was required to obtain better impedance match in a system
DDR2 RDIMM Post Register Nets

Clock Topology

Address Topology

Note: All 60 ohm Trace
DDR3 RDIMM Fly-by Clock Topology

- Outer Trace -> 60 ohm
- Inner Trace -> 60 ohm
DDR3 RDIMM Fly-by Address Topology

Note: All 60 ohm Trace
• The DDR3 data channel can run faster due to enhancements in the DDR3 component
  ‣ DDR2 ODT values reflect only: 50Ω, 75Ω, 150Ω
  ‣ DDR3 ODT values include: 20Ω, 30Ω, 40Ω, 60Ω, 120Ω
  ‣ DDR3 supports dynamic ODT
Bus Setup and Simulation

Allegro PCB SI
Bus Setup and Simulation
Bus Setup and Simulation

- PCB SI V16.0 allows you to assign models in two different ways
  1. Assign by: Model Selector
## Bus Setup and Simulation

### 2. Assign by: Component

#### Assign Bus Component Buffer Models

<table>
<thead>
<tr>
<th>Component</th>
<th>Model Selector</th>
<th>Driver</th>
<th>Active Receiver</th>
<th>Standby Receivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE2 U1</td>
<td>V48C_DQ</td>
<td>V48C_DQ_34</td>
<td>V48C_DQ_34_ODT123</td>
<td>V48C_DQ_34</td>
</tr>
<tr>
<td>MODULE2 U21</td>
<td>V48C_DQ</td>
<td>V48C_DQ_34</td>
<td>V48C_DQ_34_ODT123</td>
<td>V48C_DQ_34</td>
</tr>
<tr>
<td>MODULE1 U1</td>
<td>V48C_DQ</td>
<td>V48C_DQ_34</td>
<td>V48C_DQ_34_ODT123</td>
<td>V48C_DQ_34</td>
</tr>
<tr>
<td>MODULE1 U21</td>
<td>V48C_DQ</td>
<td>V48C_DQ_34</td>
<td>V48C_DQ_34_ODT123</td>
<td>V48C_DQ_34</td>
</tr>
<tr>
<td>NBRD U1</td>
<td>DDR3_DRIVER_DDR3_DATA</td>
<td>DDR3_DRIVER_Data_1X</td>
<td>DDR3_DRIVER_Data_1X</td>
<td>DDR3_DRIVER_Data_1X</td>
</tr>
</tbody>
</table>

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Bus Setup and Simulation

- Bus is assigned to the selected Clock or Strobe
Bus Setup and Simulation

• Derating:
Bus Setup and Simulation

- DDR2 Derating table from Micron Data sheet

Table 33: DDR2-667/DDR2-800/DDR2-1066 DS, DH Derating Values

All units are shown in picoseconds

<table>
<thead>
<tr>
<th>DQ, DQS Slew Rate (V/ns)</th>
<th>2.8 V/ns</th>
<th>2.4 V/ns</th>
<th>2.0 V/ns</th>
<th>1.8 V/ns</th>
<th>1.6 V/ns</th>
<th>1.4 V/ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS</td>
<td>△DS</td>
<td>△D</td>
<td>△DS</td>
<td>△D</td>
<td>△DS</td>
<td>△D</td>
</tr>
<tr>
<td>2.0</td>
<td>100</td>
<td>63</td>
<td>100</td>
<td>63</td>
<td>112</td>
<td>75</td>
</tr>
<tr>
<td>1.5</td>
<td>67</td>
<td>42</td>
<td>67</td>
<td>42</td>
<td>79</td>
<td>54</td>
</tr>
<tr>
<td>1.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>0.9</td>
<td>-5</td>
<td>-14</td>
<td>-5</td>
<td>-14</td>
<td>7</td>
<td>-2</td>
</tr>
<tr>
<td>DS#</td>
<td>△DS#</td>
<td>△D</td>
<td>△DS#</td>
<td>△D</td>
<td>△DS#</td>
<td>△D</td>
</tr>
<tr>
<td>2.8 V/ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.4 V/ns</td>
<td>136</td>
<td>99</td>
<td>103</td>
<td>78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.0 V/ns</td>
<td>36</td>
<td>31</td>
<td>36</td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.8 V/ns</td>
<td>136</td>
<td>99</td>
<td>103</td>
<td>78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.6 V/ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.4 V/ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- CSV format to read into Allegro PCB SI

```plaintext
# Derating table for DDR2 DQ 667/800
DQS_SLEW,0.8,1.0,1.2,1.4,1.6,1.8,2.0,2.4,2.8
DATA_SLEW,0.4,0.5,0.6,0.7,0.8,0.9,1.0,1.5,2.0
SETUP_DERATING_TABLE
  -28,12,38,50,59,67,72,139,172
  -40,0,26,38,47,55,60,127,160
  -52,12,14,26,35,43,48,115,148
  -64,-24,2,14,23,31,36,103,136
HOLD_DERATING_TABLE
  -116,-53,-11,18,41,58,72,114,135
  -128,-65,-23,6,29,46,60,102,123
  -140,-77,-35,-6,17,34,48,90,111
  -152,-89,-47,-18,5,22,36,78,99
```
DDR2 RDIMM

Post Register Timing Budget
DDR2 Post Register Simulation
Hspice Simulation

Slow Corner

Fast Corner

2113ps

1513ps
Timing Budget for DDR2 RDIMM

- Register clock to output is determined from the Simulation
- Helps in getting more accurate timing budget
- Tlsim can also be used to come up with the Timing Budget

<table>
<thead>
<tr>
<th>Timing Budget</th>
<th>Symbol</th>
<th>Setup(ps)</th>
<th>Hold(ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Period</td>
<td>tCLK</td>
<td>3000</td>
<td>N/A</td>
</tr>
<tr>
<td>Measured Delay: Clock to Actual Load</td>
<td>tPD</td>
<td><strong>-2113</strong></td>
<td><strong>1513</strong></td>
</tr>
<tr>
<td>Simultaneous Switching Adder</td>
<td>tSS</td>
<td>-200</td>
<td>N/A</td>
</tr>
<tr>
<td>*Cross Talk Adder</td>
<td>tXTALK</td>
<td>-50</td>
<td>-50</td>
</tr>
<tr>
<td>Intersymbol Interference</td>
<td>tISI</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Clock Skew</td>
<td>tSKEW</td>
<td>-150</td>
<td>-130</td>
</tr>
<tr>
<td>Register Clock Shift</td>
<td>tREG</td>
<td>-100</td>
<td>-100</td>
</tr>
<tr>
<td>DRAM Setup/Hold (derating values)</td>
<td>tISb/tIHb</td>
<td>-200</td>
<td>-275</td>
</tr>
<tr>
<td>Derating</td>
<td></td>
<td>-100</td>
<td>-94</td>
</tr>
<tr>
<td>* Register Clock Offset</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Margin (worst case corners)</td>
<td>tM</td>
<td><strong>87</strong></td>
<td><strong>864</strong></td>
</tr>
</tbody>
</table>
DDR3 RDIMM

Post Register Timing Budget
DDR3 Post Register Simulation

Address Net in Slow Corner  Control Net in Fast Corner

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI
# Timing Budget for DDR3 RDIMM

Timing Budget at 667MHz - Clock at 50%

<table>
<thead>
<tr>
<th></th>
<th>Setup (ps)</th>
<th>Hold (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>667</td>
<td>660</td>
</tr>
<tr>
<td>DRAM setup/hold @ 667MHz Clock</td>
<td>50</td>
<td>125</td>
</tr>
<tr>
<td>Timing offset for VREF error (30 mV) based on min. slew rate (30mv / 2.40 v/ns)</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>Timing offset for VREF error (30 mV) based on min. slew rate (30mv / 3.36 v/ns)</td>
<td></td>
<td>9</td>
</tr>
<tr>
<td>DRAM derating</td>
<td>88</td>
<td>50</td>
</tr>
<tr>
<td>tjit(hper) half period jitter from register</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>tQSK1 for Register (includes SSO for inverted outputs)</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>xtalk</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Margin available for Clock placement error (at 50% point)</td>
<td>250</td>
<td>310</td>
</tr>
</tbody>
</table>
Comprehensive Simulation

In Allegro PCB SI

9/17/2007
### Crosstalk Report in Allegro PCB SI

**Analysis Report Generator (case3)**

#### Standard Report | Custom Report

- **Case Selection**
  - Current Case: case1 - case2 + unknown change in 'C:\Cadence\SPF\'

- **Report Types**
  - Reflection Summary
  - Parasitics
  - Segment Crosstalk
  - Delay
  - SSN
  - Crosstalk Summary
  - Ringing
  - SDF Wire Delay
  - Crosstalk Detailed
  - Single Net ENI

- **Fast/Typical/Slow Mode**
  - Fast
  - Typical
  - Slow
  - Fast/Typical
  - Slow/Fast

- **Primary Net**
  - Net Selection: All Selected Nets
  - Driver Selection: Fastest Driver

- **Aggressor**
  - Switch Mode: Odd
  - Net Selection: All/Group Neighbors
  - Driver Selection: Fastest Driver

- **Reflection Data Simulation**
  - Reflection Measurement:
    - Comprehensive Odd
    - Pulse
    - Comprehensive Even
    - Rise/Fall
    - Comprehensive Static
    - Custom Stimulus

- **Use Timing Windows**
- **Save Circuit Files**
- **Use Reference**
- **Create Report**

---

#### All Neighbors Crosstalk Report Sorted By Worst Case Crosstalk

<table>
<thead>
<tr>
<th>Victim</th>
<th>XNet</th>
<th>Victim</th>
<th>Drvr</th>
<th>HSOddXta</th>
<th>HSEvenXta</th>
<th>LSOddXtal</th>
<th>LSEvenXtal</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 0550AA_1 A10B</td>
<td>0550AA_1 U7</td>
<td>M11</td>
<td>80.82</td>
<td>NA</td>
<td>79.57</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A15B</td>
<td>0550AA_1 U7</td>
<td>K11</td>
<td>72.43</td>
<td>NA</td>
<td>69.93</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A3A</td>
<td>0550AA_1 U7</td>
<td>F2</td>
<td>65.76</td>
<td>NA</td>
<td>62.56</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 BA1A</td>
<td>0550AA_1 U7</td>
<td>G2</td>
<td>65.14</td>
<td>NA</td>
<td>62.23</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A10A</td>
<td>0550AA_1 U7</td>
<td>M1</td>
<td>57.26</td>
<td>NA</td>
<td>53.51</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A6A</td>
<td>0550AA_1 U7</td>
<td>C2</td>
<td>51.38</td>
<td>NA</td>
<td>49.29</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 CKE1B</td>
<td>0550AA_1 U7</td>
<td>M10</td>
<td>50.14</td>
<td>NA</td>
<td>48.21</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 B2B</td>
<td>0550AA_1 U7</td>
<td>J11</td>
<td>48.79</td>
<td>NA</td>
<td>47.9</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 WEA</td>
<td>0550AA_1 U7</td>
<td>L1</td>
<td>48.45</td>
<td>NA</td>
<td>45.77</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A6B</td>
<td>0550AA_1 U7</td>
<td>C10</td>
<td>47.68</td>
<td>NA</td>
<td>45.28</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 CASA</td>
<td>0550AA_1 U7</td>
<td>N1</td>
<td>46.96</td>
<td>NA</td>
<td>44.98</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A5A</td>
<td>0550AA_1 U7</td>
<td>D2</td>
<td>42.43</td>
<td>NA</td>
<td>40.44</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>2 0550AA_1 A1A</td>
<td>0550AA_1 U7</td>
<td>F1</td>
<td>39.07</td>
<td>NA</td>
<td>37.54</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

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Crosstalk in PCB SI V. 16.0

• Comprehensive Bus Simulation
Reflection Simulation in DDR3

Reflection Simulation
Jitter=76 ps  AptACDC=1.309 ns
MinSlewSetupVAC=1.96 V/ins  MaxSlewHoldVDC=2.79 V/ins
VMACDC=164.83 mV  ArrTime=0.779 ns

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI
Comprehensive Simulation in DDR3

As an Example following settings were used to run Comprehensive Simulation:
- Geometry Window = 40 mil
- Min. Coupled Length = 50 mil
- Neighbor Capacitance = 0.01 pF

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI
S–Parameter Package Model
In Allegro PCB SI
S–Parameter

- Scattering Parameters are normally referred as S–Parameters.
- Relates to a traveling waves that are scattered or reflected when an n–port network is inserted into a transmission line.
- S–Parameter models are frequency domain and they describe the behavior of a set of ports at different frequencies.
S-parameter in Allegro PCB SI

• PCB SI V. 16.0 has:
  • DC Extrapolation Options
  • Causality
  • Passivity Check
Using Allegro PCB SI GXL

- Tlsim Engine is used for simulation.
- The converted .dml file from a touchstone file is shown here as black box with letter “S” in Sigxp.
Using Allegro PCB SI XL

- Hspice Engine is used for Simulation
- The converted .dml file from a touchstone file is shown here as black box in Sigxp
Simulation With Lumped Package Model

Lumped Package Model
Jitter=194 ps  MaxSlewSetupVAC=1.74 V/ns
MaxSlewHoldVDC=2.47 V/ns  AptACDC=2.304 ns
AptAC/DCCtr=4.637 ns  ArrTime=2.940 ns

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI
Simulation With S–Parameter Package Model

S-Parameter Package Model
Jitter=99 ps  MaxSlewSetupVAC=1.90 V/ns
MaxSlewHoldVDC=2.48 V/ns  AptACDC=2.825 ns
AptAC/DCCtr=4.485 ns  ArrTime=2.886 ns

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI
Correlation

Lab versus Simulation
DDR2 RDIMM System Verification

Lab Measurements versus Simulation Correlation on Address Net in a RDIMM DDR2 Card.

Lab Measurements

Simulation (Uncoupled)
DDR3 RDIMM System Verification

Lab Measurements versus simulation correlation on Address Net in a RDIMM DDR3 Card.

**Lab Measurements**

- Tek Stop: 10.0 GS/s
- 271 Acqs
- Slewrate of Clock = 4.2 V/ns
- Slewrate of Address = 1.7 V/ns
- Setup Region = 1.2 ns
- Hold Region = 1.3 ns

**Simulation (Uncoupled)**

- DDR3 Port Register Clock to Address Simulation
- Clock Slewrate = 4.31 V/ns
- Address Slewrate = 1.67 V/ns
- Setup Region = 1.176 ns
- Hold Region = 1.317 ns
Summary

• The challenges in designing with
  ‣ DDR2 reside in signal integrity
  ‣ DDR3 reside in timing
• Due to Tree Topology DDR2 signals arrive at the same time in every DRAM even though it has less bandwidth
• Due to DDR3 fly–by topology, timing skews exist from DRAM–to–DRAM
  ‣ therefore it is more challenging for the DDR3 controller to match timing even though it has a larger bandwidth
• Allegro PCB SI
  ‣ Can be used to design DDR3 with timing issues
  ‣ Following enhancements in 16.0 make it easy to get silicon–accurate timing data
    ▪ Comprehensive Simulation
    ▪ Slewrate derating
    ▪ Ease of use improvements with Bus Setup
CONNECT: IDEAS

CDNLive! 2007 Silicon Valley