RF-CMOS

From Spiral Inductors
to RF/Digital Systems-on-a-Chip
in 10 years

Asad A. Abidi

University of California, Los Angeles
and
LUMS School of Science & Engineering, Lahore
The Premise

• In the 1980’s and 90’s, CMOS mixed signal integration had revolutionized ICs for communications (wireline modems, wideband cable modems, disk drive read channels)

• Digital cellular telephones were emerging in the mid-1990s
  – Interim Standard (IS) 54 ratified in 1990 for digital cellular telephony in North America
  – Commercial GSM started in Europe in 1991

• Mass digital wireless devices would combine analog radio with high power DSP
RF IC Design in the mid-1990s: A Clash of Two Cultures

- Silicon
- CMOS
- Mixed Analog-Digital
- VLSI: 100K~1M transistors
- Systems-on-a-chip
- SPICE
- VHDL
- Switched capacitors
- Op amps

- Microwave
- GaAs
- Discrete components
- MMICs: 1~10 transistors
- Transmission lines
- Small-signal analog
- COMPACT
- Smith Charts
- 50 Ω
Industry vs. University
Risk-Averse vs. Venturesome

• High volumes of sales attracted semiconductor companies to wireless
• Product life cycles were expected to be < 1 year
• Radio circuit and system design was daunting; no longer part of standard university education, most radio designers worked for defence industry (or for Motorola)
• Perceived as a “black art” – exceeding conventional teaching of circuits
• Universities seized the opportunity to experiment in RF
  – Driven by desire to bring order to RF circuits – demystify the black magic
  – Implement in CMOS – (Visionary? In retrospect, perhaps, but CMOS was the only technology they could access through MOSIS)
"But Inductors are Incompatible with Silicon . . ."

4-4 SPIRAL INDUCTORS

It is almost impossible to fabricate inductors of any reasonable value of inductance in integrated circuits without resorting to additional fabrication techniques. But as the size of the spiral increases, so does the resistance of the metal pattern. The silicon wafer also contributes eddy-current losses, further degrading the $Q$. The result is that if it is at all possible, one avoids the use of inductors, substituting instead different circuit techniques to produce inductive effects.

Inductors with practical values of inductance and $Q$ are by far the most difficult components to fabricate by integrated circuit techniques—both by semiconductor and thin-film processes. Therefore, until improved results are obtained, it seems likely that any necessary inductance will be placed external to the monolithic circuit.
The Suspended Spiral Inductor on CMOS

- Eliminates substrate capacitance and substrate losses!
- Used selective etchant from early MEMs research
- Did not require extra masks; post process etch through windows

Chang, Abidi, Gaitan, 1993, UCLA

<table>
<thead>
<tr>
<th>L (nH)</th>
<th>R (Ω)</th>
<th>$\omega_0$ (GHz)</th>
<th>$Q_0$ @ 1 GHz</th>
<th>$Z_{max}$ @ 1 GHz</th>
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<td>128</td>
<td>152.5</td>
<td>2</td>
<td>5.23</td>
<td>4,300 Ω</td>
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<td>$C_p = 0.15$ pF</td>
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<td>25.3</td>
<td>23.1</td>
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<td>3</td>
<td>2</td>
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<td>$C_p = 8.4$ pF</td>
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Narrowband CMOS Tuned Circuits Become Possible

1-µm CMOS circuits now operate at 900 MHz at modest bias currents!

Common-Gate Low Noise Amplifier

Differential LC Oscillator

\[ V_{TR} + v - \]

\[ I_0 + \frac{1}{2}i \]

\[ I_0 - \frac{1}{2}i \]
Dynamic Range of MOSFETs

- MOS RF circuits show very high linearity
  - Because MOSFET does not suffer from exponential nonlinearity
  - However, at expense of lower $g_m/I$
- For RF and IF analog circuits, is MOSFET better or worse than BJT? Look at dynamic range.

\[ v_n^2 = 4kT\gamma / g_{ds0} \]
\[ \approx 4kT\gamma / g_m = 2kT\gamma \frac{V_{eff}}{I} \]

\[ \log VIP3 \propto V_{eff} \]

\[ SFDR = \left( \frac{IIP3}{N_{in}} \right)^{\frac{2}{3}} \propto I^{\frac{2}{3}}, \text{ independent of } V_{eff}. \]
MOSFETs vs. BJTs
Which is superior for RF and IF circuits?

- $I_{IP3} = -12.3$ dBm at any $V_{BE}$ for ideal BJT
- Noise set by $r'_b$
- Slide dynamic range with resistor degeneration
- $IR$ sets linearity, $R$ sets noise; like FET, dynamic range depends on bias

$g_{m(\text{eff})} = \frac{2}{R}$

Dynamic range of the MOS and BJT is almost comparable!
**Styles of CMOS Low Noise Amplifier**

**Common Gate**
- Wideband input impedance match
- Moderate noise figure (>2.3 dB)
- Robust against unaccounted parasitics

Rofougaran, UCLA, 1995

**Common Source**
- Narrowband impedance match
- Low noise figure (~1 dB at 1~2 GHz)
- Sensitive to parasitics

Shaeffer, Stanford, 1996
A Pure CMOS Downconversion Mixer

900 MHz, 1-µm CMOS
Chan, UCLA, 1993
First Generation 900 MHz Receiver Front-End

1-µm CMOS
Rofougaran, UCLA, 1995

NF=2.7 dB
The CMOS LC Oscillator

Voltage Biased

- Large voltage swing because of insulating gate; beneficial for low phase noise

\[ L_{\text{min}}(f_m) = \frac{kT \gamma \omega_0 L}{V^2_{DD}} 2Q \left( \frac{f_0}{f_m} \right)^2 \]

- Challenges
  - On-chip inductors suffer from low Q
  - Varactor for wide frequency tuning to cover process variations
Spiral Inductors on CMOS Substrates

The CMOS substrate of the mid-1990s was poorly suited to inductors:

- Many layers of thin metalization ➞ high series resistance
- Substrate doped heavily to prevent latchup ➞ large eddy current loss
Inductor-Friendly CMOS Processes Appear

- Thick metal layer to lower sheet resistance of spiral. This is uppermost layer, so planarization not an issue.

- Substrate is lightly doped to lower eddy current loss ($V^2/R$)

- Latchup prevented in other ways

- Now displacement current loss ($I^2R$) grows large

- Grounded laminated plate under inductor shields displacement currents from substrate

Yue, Stanford, 1997
Frequency Tuning: The MOSFET as Varactor

- Classic use of MOSFET as a capacitor
- As biased, FET is either in inversion or depletion
- Large oscillation sweeps across nonlinear capacitance curve; average capacitance changes smoothly

![Graph showing capacitance of a 100u NMOS varactor at 1.14 GHz](image)

Capacitance of a 100u NMOS varactor at 1.14 GHz

![Graph showing average capacitance of a 100u NMOS varactor at 1.14 GHz](image)

Average Capacitance of a 100u NMOS varactor at 1.14 GHz
Discrete Tuning of Oscillation Frequency

- Key method to compensate wide process variations in capacitance, without compromising phase noise
- Scaled FET switches do not degrade Q of tank circuit

Kral, UCLA, 1998
Is a MOS Oscillator’s Phase Noise Low Enough?

- Upconverted flicker noise very prominent in MOS oscillators
- Much worse than BJT oscillators at close-in offsets
- Far away phase noise larger because of low $Q$ on-chip inductors
- Does it matter? Only in old cellular systems such as AMPS, or in Japanese PDC
Better Understanding of Oscillator Phase Noise (1)

Circuit to Suppress Far Away Phase Noise

VCO with on-chip resonator meets demanding phase noise spec of GSM transmitter!
Better Understanding of Oscillator Phase Noise (2)

Circuit to Suppress Close-in Phase Noise

VCO with on-chip resonator meets the close-in phase noise of PDC receiver!

Ismail, UCLA, 1993
Architectures Fit for Highly Integrated Receivers

Zero IF

• More than any past imperative, CMOS in RF has propelled the widespread use of direct conversion to zero IF

• Works well with highly linear active CMOS filters for channel selection

Digital FSK Detector

900 MHz

I

Q

Zero IF

900 MHz

VCO

DC offset

Signal

1/f noise

• DC offset and flicker (1/f) noise are major issues – which have been overcome with DSP or analog methods
Architectures Fit for Highly Integrated Receivers

Low IF

• A way to avoid DC offset and 1/f noise, and use low frequency circuits after downconversion . . .

... but now with the need to suppress an image coincident in frequency

• Conventionally image is filtered pre-mixer. With high RF and low IF, the filter cannot be integrated on-chip.

• Post-mixer image rejection must distinguish between positive and negative frequencies; represent signals in quadrature phases
Image-Reject Filters: Passive & Active

Crols, KU Leuven, 1995
900 MHz WLAN CMOS Transceiver
UCLA 1997

- One of the first WLAN transceivers in the 900 MHz ISM band (FHSS, 4-FSK)
- Highly integrated, with on-chip low-output Power Amplifier
- Fully differential signal path
- On-board 100 MHz logic for direct digital frequency synthesizer
- 1-µm CMOS, TX: 100 mA, RX: 120 mA from 3V
- 8.6 dB NF, –8 dBm IIP3, direct conversion
1.9 GHz CMOS Receiver
UC Berkeley, 1997

- Intended for cordless telephone applications
- Integrates pipelined ADCs
- Weaver receiver suppresses image
- 0.6-µm CMOS, 67 mA, 3.3V
- –90 dBm sensitivity, –7 dBm IP3
900 MHz GSM RX and TX
UCLA 2001, 2002
Commercial CMOS GSM Cellular Chipset

Silicon Laboratories 2001

• Supports multiple bands: GSM 850, 900, DCS 1800, PCS 1900
• Low IF to 100 kHz, followed by digital filtering and analog interface at zero IF
• Offset PLL transmitter
• Three chip solution

“Silicon Laboratories: Raising CMOS to the Power of RF”
Monolithic Bluetooth Wireless System-on-a-Chip
Alcatel 2001

- 2.4 GHz ISM band; low IF RX to 1 MHz (Bluetooth makes this easy)
- 2 Mb Flash, 48k SRAM, ARM7, UART
- 0.25-µm CMOS
- Modelled substrate coupling, shielding, clock timing
Bluetooth SOC
Ericsson 2002

- 75 kgate microprocessor, 256k RAM
- Receiver: Low IF of 1 MHz
- Differential RF and analog signal path
- Substrate coupling modelled; p-well ring

- Inductorless circuits, except for oscillator
- 0.18-µm CMOS, –78 dBm sensitivity, –14 dBm IIP3, 30 mA RX, 30 mA TX, 5.5mm²
Atheros 802.11a/b/g SOC ca. 2006
Infineon GSM CMOS SOC ca. 2006
TI GSM 90nm CMOS SOC ca. 2005

Digital

Memory

RF

Analog
Spurious tones – how to eliminate?

**Generation**
- Supply blocking of digital blocks → high cap. filler cells
- Optimize external blocking caps
- Scale down digital gates wherever possible

**Sensor**
- Substrate guard rings
- Differential structures
- High quality on-chip-supply blocking
- Optimize external blocking caps

**Coupling**
- High Ohmic substrate (20Ωcm)
- Separate sensitive from noisy grounds
- Separate sensitive from noisy blocks (floor-planning → moat rings)
The Need

Quad-band GSM
GPRS
Wideband CDMA
EDGE
GPS
Bluetooth
802.11b ...

Cram down the funnel of functions

• Large number of independently developed radio boards, all squeezed into a small mobile device ...
• You see one antenna, there are actually 3 or 4 ...
• Next month there will be a new wireless application
• Where will this end??
The Software Defined Radio

- Ultimate in flexibility!

- Needs 12b, 10 GS/s A/D Converter (ADC)

- Low power solution not in sight, Moore’s law doesn’t help

- [Walden, IEEE JSAC 99]
Lowpass Sampler w/ Internal Anti-Alias

[Yuan, 2000]

Rectangular Window Integration

- Main-lobe passes wanted signal at DC
- Side-lobes roll off with 20 dB/decade
- Notches @ nf_s for anti-aliasing
- Wider stop-band with higher f_s

Windowed Integration Filter Response

\[
|H(f)| = \frac{g_m T_s}{C} \left| \frac{\sin(\pi T_s f)}{\pi T_s f} \right|
\]
Filter Realization

From mixer $g_m$

2.5~10mS

$C_{IIR}$

D-T Pole

Sinc

$2 + 4$

To A/D Converter

$C_u = 200f\sim 1.6pF$

11g, GSM

$C_{IIR} = 25C_u, 200C_u$

$C = C_u, 2C_u$

GSM Gain 6~36 dB

11g Gain -4~26 dB
On-chip Selectivity
Displaces RF preselect filter

Filter specification (WCDMA Band)
- $f_s = 480 \text{ MHz}, 4\downarrow & 3\downarrow, f_{ADC} = 40 \text{ MHz}$

Wanted 802.11g channel
- $f_s = 480 \text{ MHz}, 4\downarrow & 3\downarrow, f_{ADC} = 40 \text{ MHz}$

Measured response

Spurious Response
- 802.11g: -60dBr
- GSM: -74dBr

Currents from 1V
- 802.11g Idc: 13~28 mA
- GSM Idc: 8~23 mA
Final Clock-Programmable SDR Receiver

- RX tolerates AM blockers as high as -20dBm with no preselect filter
- Still higher linearity is needed from LNA and mixer

Full RX Chain Summary

<table>
<thead>
<tr>
<th></th>
<th>GSM</th>
<th>802.11g</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF (High Gain) [dB]</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>IIP3 (Mid Gain) [dBm]</td>
<td>-3.5</td>
<td></td>
</tr>
<tr>
<td>IIP2 (Mid Gain) [dBm]</td>
<td>+65</td>
<td>+67</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>18-52</td>
<td>23-57</td>
</tr>
</tbody>
</table>
A “Digital” RF Transmitter
Challenges Ahead

• How to design and simulate?
  – Narrowband RF, and
  – Continuous-time analog, and
  – Discrete-time analog, and
  – Digital

• How to devise new architectures?

• How to predict on-chip couplings?

• How to package these chips?