Design challenges of large mixed-signal ASICs with hierarchical segmentation.

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Introduction: mixed signal ASICs

- The world is still rather ...
  - analog than digital
  - time-continuous than time-discrete.
  → quantization and sampling

- Mixed-signal designs connect analog and digital domains
  - e.g. ADCs and DACs
  - separate digital and analog blocks
    - design, simulation, layout
  - floorplanning with large blocks
  - put together at “chip assembly”
Problem: top-level blocks vs. hierarchy of mixed cells

- mixed-signal designs with regular structures
  - Camera chips
  - Field Programmable Analog Arrays
  - Nerve stimulation controllers
Example: Epiretinal Stimulator

Glasses with PA, prim. coil and LED

Array of gold electrodes attached to retina

Glasses with PA, prim. coil and LED

Array of gold electrodes attached to retina

Chip Implant

- ASIC with 232 stimulation electrodes
- AMS H35 technology
  - 0.35µm, 50V CMOS
  - >100k Gates
- Energy and clock recovery
- Full duplex com.
- Safety features
- Power control

- Total 232 electrodes
  - 3.2µ-1mA, max. ±15V
  - Active charge balancer
  - mixed-signal leaf-cell
- Hierarchy of mixed cells
Field Programmable Analog Array

- Reconfigurable analog filter with time-continuous signal processing.

- Analog transfer-function
  - Analog signal (0.1 - 250 MHz)
  - Processing through filter on FPAA
  - Spectrum Analysis or A/D conversion

- Digital logic for filter reconfiguration
  - Graphical entry of configuration on PC through MATLAB toolbox
  - Download via USB/JTAG interface to chip
  - Setting of digital configuration memory
  - Instancing of filter on FPAA
FPAA structure

- **Hexagonal Structure**
  - provides configurable signal routing between cells
  - enables parallel connection
  - allows all orders of feedback
  - arbitrary filter structures possible

- **Each cell has**
  - One input node
  - multiplexer for 6 branches + 1 self-feedback
  - Each branch is a digitally tunable transconductor
  - Each branch has an inverting and non-inverting output
FPAA Layout (bottom level)

- 6 switchable transconductance amplifiers
- reference-voltage current-mirrors
- digital configuration logic
FPAA Layout  (intermediate level)

- 7 tunable transconductance amplifiers (branches)
- common-mode feedback circuit, analog output buffer
- analog and digital routing
FPAA Layout (top level)

- 7 configurable analog blocks
- reference-voltage current-mirrors
- digital configuration logic
- padring IOs
- analog and digital routing
- logos

- UMC 130nm
- approx. 50,000 analog transistors
The Methodology Maze

- Virtuoso
- floorplanning
- Encounter
- hierarchy
- netlist
- schematic
- AMS-simulation
- LVS & DRC
- analog RCX
- digital timing

Introduction
Examples
Methodology
Implementation
Conclusion
Analog vs Digital Flow

- **analog**: DFII, Virtuoso
  - netlisting: schematic
  - placement: arbitrary, p-cells
  - routing: full-custom, hand-drawn
  - simulation: analog, Spectre
  - verification: DRC, LVS, RCX

- **digital**: IUS, Encounter
  - netlisting: VHDL, Verilog
  - placement: standard-cell abstracts, grid
  - routing: automatic, scripted
  - simulation: digital, NCsim
  - verification: + timing analysis

- **which flow for assembly of mixed-signal cells?**
Assembly of Mixed-Signal Cells

◆ things to be considered  (decisions made for this particular design)
  – analog designkit is reference for tapeout
  – digital designkit faulty, uses different layer table
  – most of the chip-area is analog devices, take advantage of Virtuoso features
  – full-custom place and route, hand-drawing ability, “feeling” for symmetry
  – hierarchy of schematics rather then HDL-netlists
  – analog or AMS simulation integrated in IC-package

◆ DFII and Virtuoso seems to be the way

◆ issues to address
  – export digital layouts from Encounter to Virtuoso
  – connection of analog and digital netlists
  – digital global routing, clock tree synthesis
  – global timing analysis
Export from Encounter to Virtuoso

- **layout data**
  - metal lines (DRC)
  - pins (LVS)
  - vias with different orientations as instances
  - standard-cells as abstracts
  - pin metal and local routing of standard-cells

- **LEF/DEF**
  - comprehensive data format for layout and netlist
  - standard-cells are imported from library LEF
  - layer table of analog and digital design kit don’t match
    - ASCII file -- patch possible but cumbersome

- **GDS II**
  - standard-cells are included
  - layers can be matched by mapping-table at streamout
  - netlist has to be imported separately

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**AMS Hierarchy Editor**

- mixed-signal simulation needed for verification
  - co-simulation of digital configuration input and analog behaviour

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AMS simulation

- mix of simulations:
  - transient simulation for serial configuration data shift-in
  - AC simulation for check of analog behaviour over frequency sweep

- previous operating point
  - use operating point after transient simulation for AC simulation
Global netlist

- global LVS check of mixed-signal design
  - import Verilog netlist after layout into Virtuoso
  - hierarchical modules are translated into schematics
  - standart-cells become abstract and functional views
Digital top level

- Distributed digital parts
- Clock tree synthesis
- Buffers
- Antenna-Diodes

- Digital hierarchy hidden in Virtuoso schematics

- Automated CTS and timing analysis
  - back to Encounter?
  - netlists to Verilog
  - GDS export
  - return to Virtuoso?

- For simple digital parts, it could be done by hand
  - balanced, symmetrical control signal routing
  - precautionary placement of buffers and antenna-diodes
Digital timing signoff

- No global digital netlist
- No global digital timing analysis
- Make bottom-level insensitive to clock skew
  - similar to JTAG, introduce extra flip-flops to avoid hold-violations
  - data signal inputs are latched at rising clock edge
  - data signal outputs change at falling clock edge

- Timing within bottom-level blocks verified
- Data has half clock-cycle to move to next stage.
  - hold-violations between distant registers avoided by lower clock frequency

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Conclusion

◆ The Good
  – feasible design-flow for mixed-signal ASICs
  – AMS simulation, transient and AC for functional verification
  – LVS and DRC for verification of layout
  – most of it is done in Virtuoso, circumvent bad digital designkit
  – very easy and effective for modest digital parts

◆ The Bad
  – digital parts need a lot of manual adaptation
  – many benefits of digital automation can not be used

◆ The Remainder
  – more digital-centric designs could benefit from Encounter as top-level tool
    • sophisticated scripting needed to resemble full-custom analog design
    • some analog features would be missing
  – bottom line:
    • mixed blocks in one level is straightforward
    • hierarchy of mixed-signal cells is problematic
    • still two separate flows with different tools
    • looking forward to OpenAccess database, IC 6.1
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