



cadence®

Cadence Training Brochure  
2012 - 2013

Over the last few years, a few major trends have emerged in the way that students prefer to consume training. One trend is toward training that is delivered “virtually.” This is driven by two macro-economic changes. The first is that tight operating budgets have reduced allocations available for student travel to a single site for training. The second is that design cycles have become so tight that students struggle to leave their worksite for multiple days at a time.

Another emerging social trend is that students want to receive their training right when they need it, without delay, wherever they need it, and only to the extent that they need at any given time.

At Cadence, we have implemented several ways to receive training beyond the traditional classroom model.

First, we have enabled live delivery of virtual training through the Internet with our Virtual Classroom option. No part of the live delivery is compromised as you have a live instructor, electronic documents are still received, and labs are still performed using an online environment.

Second, we have vastly expanded our Internet Learning Series [iLS] of self-paced training. This way the student can take the training when they have the time and at their own pace.

Finally, we have implemented a subscription model where students can gain year-long access to any of the online training available for a product platform. They can use as much training from the collection of classes as they like, using them whole or in parts, defining their own paths, and meeting their own needs.

Training must adapt to the individual needs of the student, and Cadence has implemented world-class training and delivery solutions to meet those needs.

Let me invite you to now browse through our brochure to discover the world of Cadence® Training. Thank you for being our customer!

Scott Hargraves  
Group Director, Global Training Services

**Table of Contents**

Training Options.....3

Internet Learning Series [iLS] and iLS Subscription .....4

Virtual Classroom [VC] .....5

Methodology-Based Language Training .....6

Digital Verification, Languages, and Methodologies with Incisive Technology .....8

Digital Design with Encounter Technology ..... 10

PCB and Package Design with Allegro Technology ..... 12

Custom Design with Virtuoso and DFM Technology..... 14

# Training Options

## Categories

### Tool

We offer more than 130 classes ranging from Basic to Advanced to Language and Methodology. The focus of Tool training is usage and how to access technology effectively. Basically, Tool training is considered everything that is not categorized Advanced or Language and Methodology.

### Advanced | Engineer Explorer [EE]

The Engineer Explorer Series is designed for more experienced users of Cadence tools. The objective of each offering is to increase your productivity, providing more sophisticated strategies, tool exploration, and learn-by-doing techniques.

### Language and Methodology

Language and Methodology courses include design theory/ language theory and techniques. You will find technical capabilities combined into a consistent and repeatable flow.

## Delivery methods

### Instructor-Led | Live

We provide Instructor-Led classes that are offered at our worldwide training centers, at your site, or through the Virtual Classroom.

### Internet Learning Series [iLS] | Self-Paced

iLS are self-paced Cadence courses delivered over the web. With iLS you proceed at your own pace, anytime and anywhere. iLS includes dynamic course content, hands-on downloadable labs, instructor notes, tool demonstrations, self-assessments, audio explanations, and online support. Learn more about iLS on page 4.

### Virtual Classroom [VC] | Live-Remote

Virtual Classroom offerings use the exact same content and same expert instructors as our Live classes in a remote environment. You will dial into a conference call to hear the lectures, use remote labs, and get help from the instructor who can monitor your progress and answer your questions, as you would do in a conventional classroom – except, you do it from the convenience of your desktop. Learn more about VC on page 5.

## Delivery locations

### Public

Public training is available in our state-of-the-art classrooms at our worldwide training centers. To view our current pre-defined schedules please visit [www.cadence.com/training](http://www.cadence.com/training).

### Onsite | Private

Onsite classes are held at your site including flexible scheduling. Onsite training provides a private learning experience for your team with discussions centering on your unique design needs.

## Training contents

### Standard

Our Standard training courses are developed with pre-defined sets of topics. Hands-on exercises give you a chance to experiment with the tools and practice concepts covered during lectures.

### Tailored

In addition to Standard training courses, Tailored courses offer you the option to mix, add, or eliminate topics from one course or multiple courses. No new material is created for a Tailored course, and the Standard course database is used.

### Customized

Customized training provides you with maximum flexibility when it comes to training on Cadence products. You can request only certain topics to be covered, or request new topics to be added; you can even provide your own design or database to use in the labs.

# Internet Learning Series [iLS] and iLS Subscription

## What is iLS?

Internet Learning Series [iLS] are self-paced EDA classes delivered over the web that let you proceed at your own pace, anytime and anywhere.

iLS includes dynamic course content, hands-on downloadable labs, instructor notes, tool demonstrations, self-assessments, audio explanations, and online support.

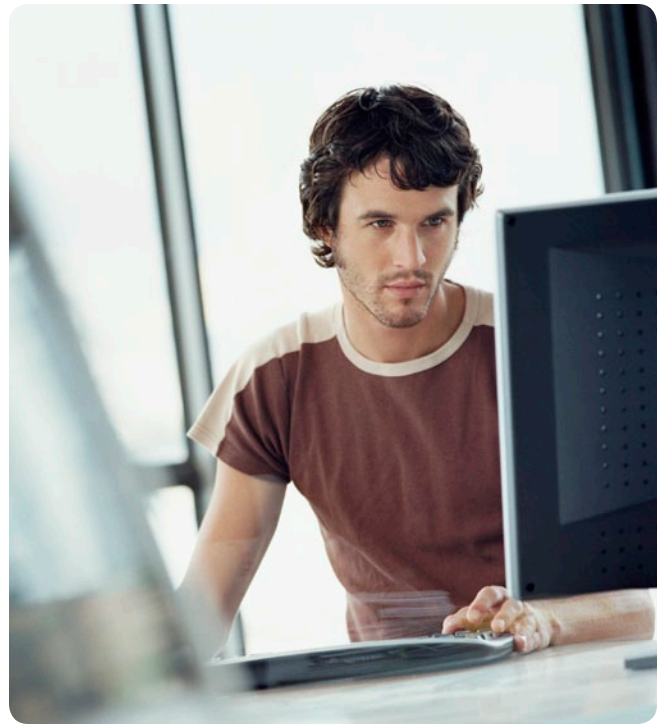
## Advantages of iLS

- Allow you to proceed at your own pace, anytime and anywhere → ultimate flexibility.
- Provide a convenient and cost-effective training solution → no need to travel.
- Enable individual engineers or even design teams to be more productive early in the design cycle → no need to wait for a public class or schedule a private class.

## iLS Offerings

We have two program offerings for iLS courses:

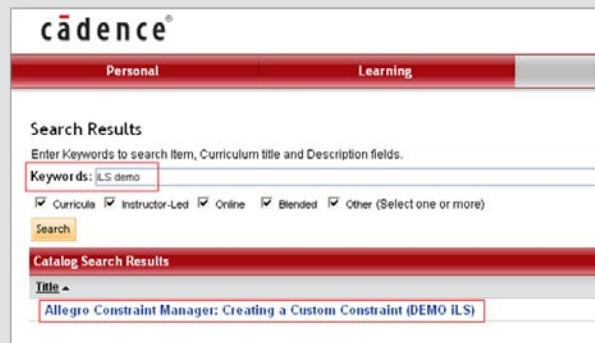
1. Our **single user program** is available for six months as a per customer use model.
2. If you are interested in two or more iLS courses, consider the **Online Training Subscription**, which provides an easy and cost-effective way to access all the online offerings (courses, books, recordings, update training) in one or more of the four technology collections. Your subscription will be for a period of one year per user license.



An Online Training Subscription helps you get the most out of your Cadence investment by allowing you to subscribe to an entire technology collection. Contact your training coordinator for more details.

## How to Preview an iLS Course

1. First log in to the Cadence Learning Management System (LMS): <https://cadence.plateau.com/plateau/user/ssoLogin.do>
2. Search for 'iLS demo'
3. Click on 'Go to Content' for the Allegro Constraint Manager: Creating a Custom Constraint (DEMO iLS)
4. Agree to the 'Cadence License Agreement' and start the free module on Allegro Constraint Management - learn how iLS works independent to the subject of your interest.



# Virtual Classroom [VC] Live Remote Training

## Why Choose Virtual Classroom Training?

- Cost-effective and time-efficient
- Efficient multi-site training across geographic regions
- Four-hour sessions leave the rest of each day free for you to concentrate on your design projects

## What is a Virtual Classroom?

A Virtual Classroom is a web-based environment that allows you to participate in live training events without the need to travel.

You listen to lectures, participate in lab exercises, ask questions, and receive feedback just as you would do in a conventional classroom—except you do it from the convenience of your desktop or anywhere you have an Internet and phone connection. It saves you expense and travel time.

Each course is usually divided into four-hour sessions spanning several days. Each session consists of lectures and lab exercises using Cadence software. Between sessions, you can further explore the lab exercises on your own.

## Four Easy Steps to Participate in a Virtual Classroom Training

1. Use a compatible OS such as Linux or Windows
2. Use a compatible browser such as Internet Explorer or Firefox
3. Install RealVNC Viewer, Java, and Imera TeamLinks software
4. Call in to the audio conference - you can ask questions during a virtual class by either using the meeting interface or by phone.

## Where to find a Virtual Classroom

1. Go to <http://www.cadence.com/training>
2. Select your regional course catalog
3. Select Virtual Classroom from the top menu

“Virtual training is a necessity in today’s working environment. Cadence Virtual Training allows for teams located across the globe to take the same class simultaneously, without the cost or burden of traveling. More employees have the opportunity to take a variety of classes and the convenience of flexible class times. They still benefit from student-teacher interaction, as well as interaction among the students. IBM operates in a globally integrated environment that demands this kind of virtual education.”

Susan Benysh, Ph.D., PMP  
IBM Corporation  
Rochester, Minnesota, USA

# Methodology-Based Language Training

Worldwide leaders in Methodology-based language training for electronic design

## What Sets us Apart from Other Training Providers

- Expert developers, experienced trainers
- High-quality, standards-based content
- Open-minded, flexible approach
- Innovative, up-to-date course materials
- The latest remote learning options
- Worldwide training centers

## Where to Find our Offerings

[www.cadence.com/training](http://www.cadence.com/training)

- Education is our sole mission. This focus and commitment has allowed us to develop a style of training that gives you the best possible return on your investment with us.
- We offer a variety of industry-renowned classes on languages and methodologies.
- Design, verification, assertion and scripting languages such as SystemVerilog, VHDL, SystemC™, TLM, C-to-Silicon Compiler, Specman® *e*, Perl, and Tcl, and methodologies such as the UVM.

## Why Verification using Specman *e*?

*e* is more than just a verification language. *e* is the verification language with a built-in verification methodology.

The benefits of using *e* as a functional verification language:

- A specialized, standardized IEEE language designed for functional verification
- An easy and intuitive language with a high ROI
- A proven built-in verification methodology (*e*RM, which is at the core of UVM-*e*)
- A mature and thriving ecosystem with a large code-base of Verification IP and libraries

### Course Catalogue

View: **Instructor-Led Courses** | Online Courses | Virtual Classroom

- Advance with Engineer Explorer Series
- Custom IC Design – Virtuoso
- Digital IC Design – Encounter
- Functional Verification – Incisive
- **Specman**
  - Specman Fundamentals for Block-Level Environment Developers
- Language Courses for PLD, ASIC and PCB Design
- **SystemVerilog**
  - SV3-SystemVerilog Advanced Verification Using UVM
- Manufacturability
- Previews of Education Services Classes
- System Interconnect Design – Allegro & OrCAD

Our Cadence *e* training classes will get your verification engineers jump-started with the knowledge and experience of more than 10 years of innovation and success.

“The Cadence Specman training is a great way of learning the *e* language, the Specman tool, and the Universal Verification Methodology (UVM). The training is a great experience with skilled trainers who have real-world verification experience and cater to the needs of every participant.

The well-rounded combination of theory and hands-on exercises make the Cadence training a unique learning experience that helped increase my team’s functional verification productivity and, as such, I highly recommend this Cadence training.”

Raimund Soenning, Fujitsu Semiconductor Europe GmbH



“I have a dream: I can reuse my favorite testbench in every new project and.....This dream came true after the Cadence UVM class!”

Joerg Keber, CAD Support Engineer, NXP Semiconductors Germany GmbH

[www.esperan.com](http://www.esperan.com)

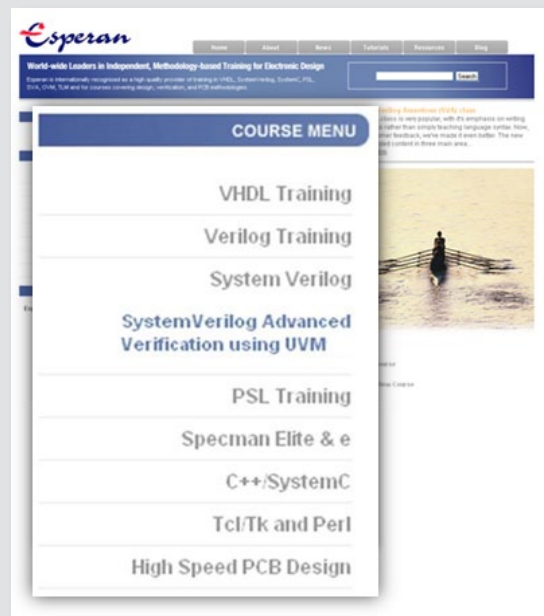
With a special focus on practical application, IEEE standards, and industry best-practices, Esperan (a Cadence company) has been developing and delivering tool-independent language and methodology training for the electronics design industry since 1993.

### Why Verification using the UVM?

The UVM is a SystemVerilog class library of essential verification building blocks and a methodology for using these blocks to create powerful, reusable and configurable verification environments.

The benefits of using the UVM:

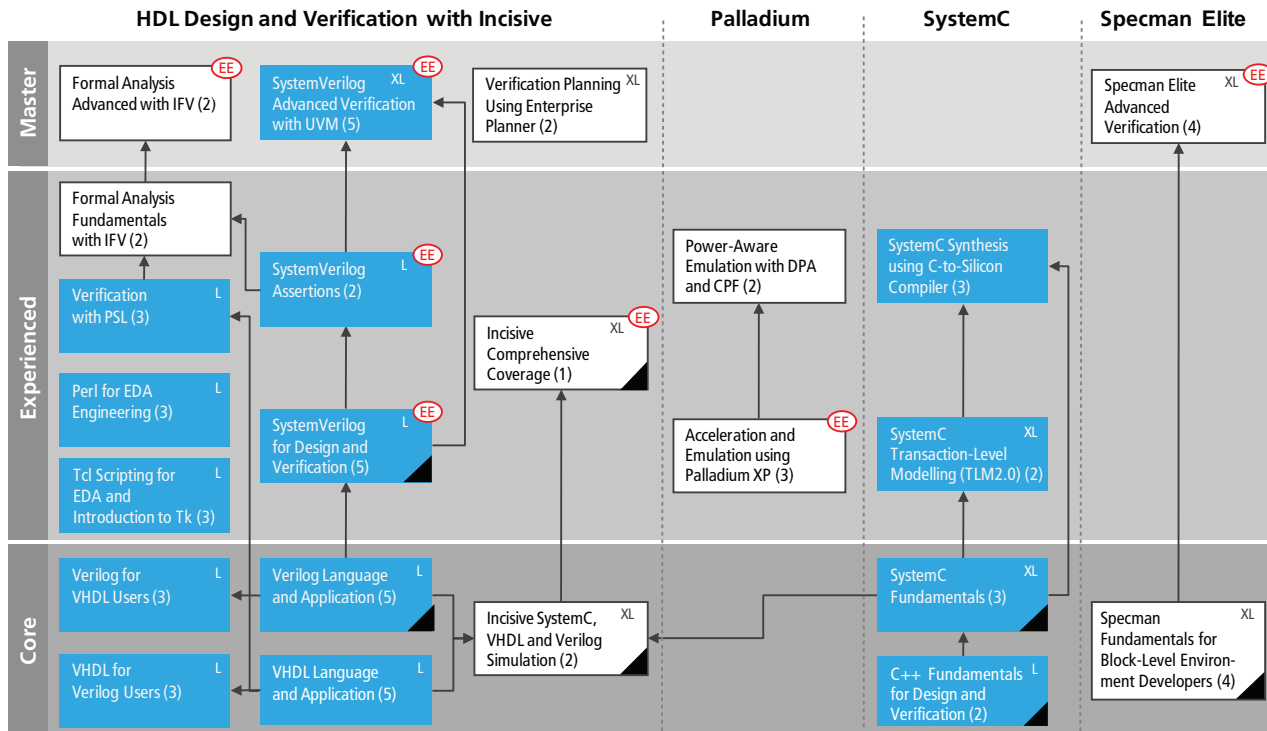
- No new language or syntax to learn – class library based on standard IEEE1800 SystemVerilog
- Open source, vendor-independent, and supported by all major simulation tools
- Verification building blocks developed with familiar object-oriented design techniques
- A proven verification methodology based on more than 10 years of success
- A thriving and growing base of Verification IP and libraries



Our **SystemVerilog Advanced Verification using UVM** training class will get your engineers creating high-quality verification components in the shortest possible time.

# Digital Verification, Languages, and Methodologies with Incisive Technology

## Learning Maps



▲ Also available as a self-paced course (EE) Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#)

□ Cadence Incisive trainings    ■ Methodology-based language training

## Course Descriptions

### HDL Design and Verification

**Verilog Language and Application:** This course provides a solid background in the use and application of Verilog to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.

**VHDL Language and Application:** This course provides a solid background in the use and application of VHDL to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.

**Formal Analysis Fundamentals with Incisive Formal Verifier:** This course introduces the principles of formal analysis (FA) and teaches methodology and techniques to enable the most efficient use of Incisive® Formal Verifier. The course provides an excellent jump start for design and verification engineers, with no prior knowledge of FA, to become immediately effective.

### Formal Analysis Advanced with Incisive Formal Verifier:

This advanced course follows on from the Formal Analysis (FA) Fundamentals class to address complex issues that can reduce performance. The course examines more advanced FA methodology and tool features, including links to verification planning and management.

**Verification with PSL:** This course provides a deep introduction to PSL, followed by guidelines and methodologies for describing and debugging complex design assertions for verification, coverage, and formal analysis (FA).

### SystemVerilog

**SystemVerilog for Design and Verification:** This course gives you an in-depth introduction to the main enhancements SystemVerilog adds to Verilog. The course discusses the benefits and issues with the new features and demonstrates how design and verification is more efficient and effective when using SystemVerilog constructs. In particular, the course covers key verification features for randomization, coverage, assertion checking, and object-oriented design.

**SystemVerilog Assertions:** This course gives you an in-depth introduction to SVA, together with guidelines and methodologies to help you create, manage, and debug effective assertions for complex design properties.

**SystemVerilog Advanced Verification using UVM:** UVM (Universal Verification Methodology) is a class-based verification library and reuse methodology for SystemVerilog class library. This course describes the verification building blocks and infrastructure provided by UVM, and defines a methodology for creating verification environments with reusable UVM Verification Components (UVCs). This course also contains an optional review of SystemVerilog class constructs, together with an overview of object-oriented concepts and features.

## Simulation and Coverage

**Incisive SystemC, VHDL, and Verilog Simulation:** This course addresses Incisive mixed-language (SystemC, VHDL, and Verilog) event-driven digital simulation. The course steps you through compilation, elaboration, simulation, and analysis, explaining the most popular options at each step.

**Incisive Comprehensive Coverage:** This course explores Incisive comprehensive coverage features, with which you can measure how thoroughly your testbench exercises your design. The course addresses coverage of SystemC, VHDL, Verilog, and mixed-language designs.

## Emulation and Acceleration

**Acceleration and Emulation with Palladium XP:** This course introduces you to using the Palladium® XP verification computing platform for accelerating the verification of design. The course steps you through preparing a design for emulation, running a simulation, debugging the results, and improving simulation performance.

**Power-Aware Emulation with DPA and CPF:** This course shows you how to use Palladium XP for dynamic power analysis (DPA) and power-shutoff system verification using the Common Power Format (CPF).

## SystemC/C++

**C++ Language Fundamentals for Design and Verification:** This course provides an introduction to the C++ programming language for those that will use C++ for design or verification. During class, you write and execute C++ code that includes C++ classes, member variables and functions, constructors, destructors, inheritance, and polymorphism.

**SystemC Language Fundamentals:** This course teaches the IEEE standard 1666-2005 SystemC language and explores how it can be used for system, hardware, and verification modeling.

**SystemC Transaction-Level Modeling (TLM 2.0):** This course teaches the OSCI® SystemC TLM 2.0 library. The TLM 2.0 library provides model interoperability for memory-mapped SoC platforms. The library addresses the use cases of software application development and hardware/software integration, software performance analysis, hardware architecture analysis, and hardware functional verification.

**SystemC Synthesis using C-to-Silicon Compiler:** This course introduces hardware designers to high-level synthesis. It introduces them to the SystemC language, examines the SystemC coding style for high-level synthesis, and explores micro-architectural alternatives in the context of the Cadence C-to-Silicon Compiler.

## Specman Verification

**Specman Fundamentals for Block-Level Environment Developers:** This course is an introduction to the *e* language and the Incisive Enterprise Specman Elite Simulator product. The course is based on a coverage-driven verification methodology, which is applicable for a broad range of designs. The course shows how to create a reusable, block-level verification environment and then how to instantiate, customize, and write tests for this environment. The verification methodology taught by this class is compatible with the Universal Verification Methodology (UVM).

**Specman Elite Advanced Verification:** This advanced course follows on from the Specman Fundamentals class to provide a much greater understanding of the *e* language and the Specman tool. This course covers advanced language and tool techniques and examines how to scale verification environments from a block to system level while obtaining maximum reuse of your Verification IP.

## Metric-Driven Verification

**Verification Planning using Enterprise Planner:** This course teaches how to build a verification plan using Incisive Enterprise Planner giving special attention to the planning process and the need for rigorous planning. All aspects of Enterprise Planner are discussed.

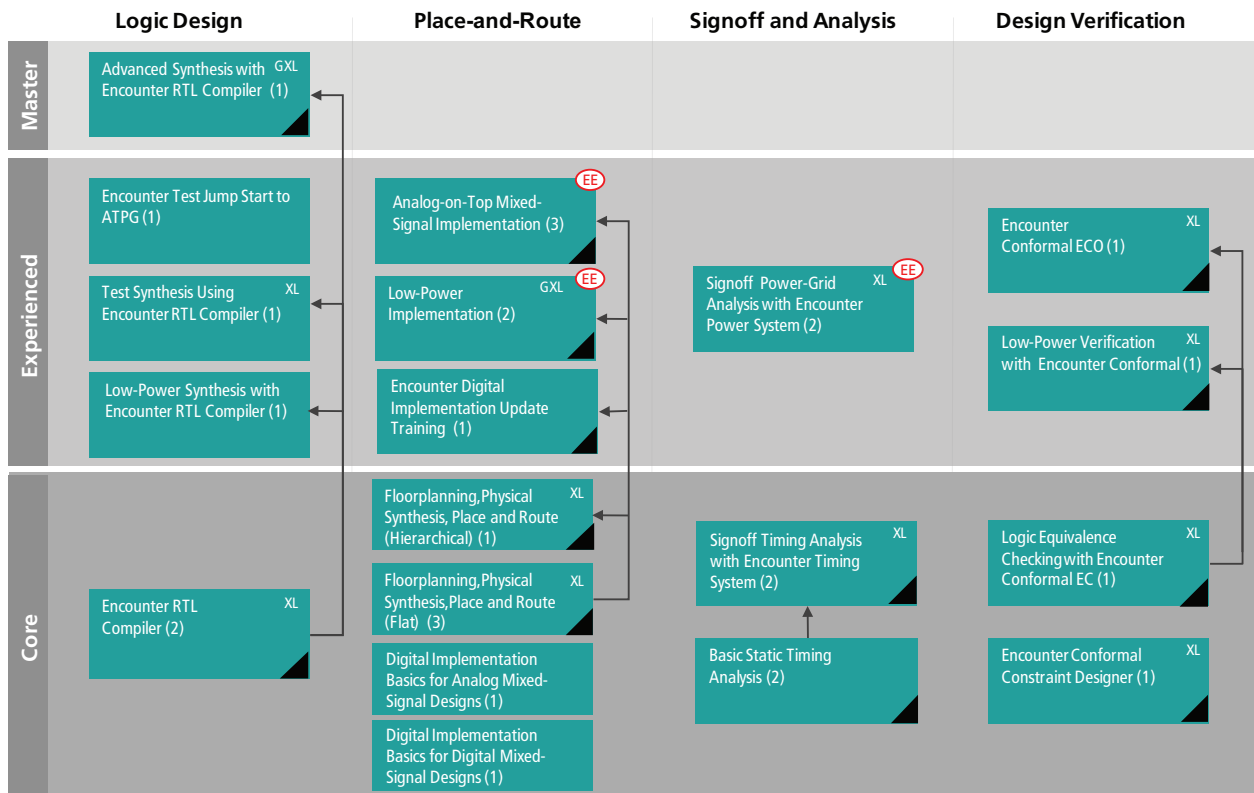
## Scripting

**Tcl Scripting for EDA + Intro to Tk:** This compact course is the fastest and most effective method for engineers to understand the potential of Tcl and become proficient in the language. The Tk part teaches fundamental concepts like how to create widgets, how to lay them out, and how to “bind” new behaviors to events.

**Perl for EDA Engineering:** This course was written from the ground up with EDA professionals in mind. It teaches both basic and advanced concepts of Perl for processing large volumes of data, translating tool output formats, and assisting in general shell and tool tasks. This course is invaluable to anyone working with Perl scripts on a regular basis.

# Digital Design with Encounter Technology

## Learning Map



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## Course Descriptions

### Logic Design

**Encounter RTL Compiler:** In this course, you explore the features of Encounter® RTL Compiler with global synthesis technology. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, optimize for low power, and interface with other tools.

**Advanced Synthesis with Encounter RTL Compiler:** In this course, you use Encounter RTL Compiler global synthesis to debug problems in the synthesis of complex designs when optimizing for timing, area, and power.

**Low-Power Synthesis with Encounter RTL Compiler:** In this course, you use Encounter RTL Compiler with global synthesis to lower power consumption through single-pass multi-Vth optimization, hierarchical and multi-stage clock gating, multi-supply voltage (MSV) support, power shutoff, and state-retention power gating.

**Test Synthesis using Encounter RTL Compiler:** In this course, you learn to use Encounter RTL Compiler to insert test structures in your design, synthesize for test, and connect scan chains.

**Encounter Test Jump Start to ATPG:** In this course, you learn to use Encounter True-Time ATPG for static automatic test pattern generation.

### Place and Route

**Floorplanning, Physical Synthesis, Place and Route (Flat):** In this course, you explore high-level design planning and implementation by using Encounter Digital Implementation (EDI) system software. You will learn several techniques for floorplanning, placement, detail routing, and optimization while implementing timing closure strategies.

**Floorplanning, Physical Synthesis, Place and Route (Hierarchical):** In this course, you explore the features of EDI system software for creating and implementing a hierarchical design.

**Low-Power Implementation:** In this course, you synthesize and implement several low-power techniques to reduce both dynamic and leakage power during logic synthesis implementation.

### **Digital Implementation Basics for Analog/Mixed-Signal Designs:**

In this course, you learn the basics of digital implementation for analog/mixed-signal designs by using EDI System software. You explore floorplanning, placement, power planning, clock-tree synthesis, timing optimization, and detail routing.

### **Encounter Digital Implementation Update Training:**

The update training focuses on the most important changes in the software features from the previous version (9.1). Topics range from floorplanning through placement and design verification.

**Analog-on-Top Mixed-Signal Implementation:** In this course you learn an in-depth approach to implementing an analog and digital mixed-signal design. You use Virtuoso® Layout XL/GXL, EDI System software, NanoRoute® router, and Virtuoso Space-Based Router (VSR) for primary and assembly routing.

## **Signoff and Analysis**

**Basic Static Timing Analysis:** In this course, you learn the basic concepts of static timing analysis and apply them to constrain a design.

### **Signoff Timing Analysis with Encounter Timing System:**

This course is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Encounter Timing System.

### **Signoff Power-Grid Analysis with Encounter Power System:**

In this course, you explore the need for power-rail analysis and use the Encounter Power System power consumption and power rail verification software to run several types of power-consumption and power-rail analyses.

## **Design Verification**

**Encounter Conformal Constraint Designer:** In this course, you use Encounter Conformal® Constraint Designer to manage constraints for complex SoC designs from RTL through layout.

### **Logic Equivalence Checking with Encounter**

**Conformal EC:** In this course, you use the Encounter Conformal Equivalence Checker to perform functional verification. You learn the basic flow of equivalence checking and how to run hierarchical comparison of designs.

### **Low-Power Verification with Encounter Conformal**

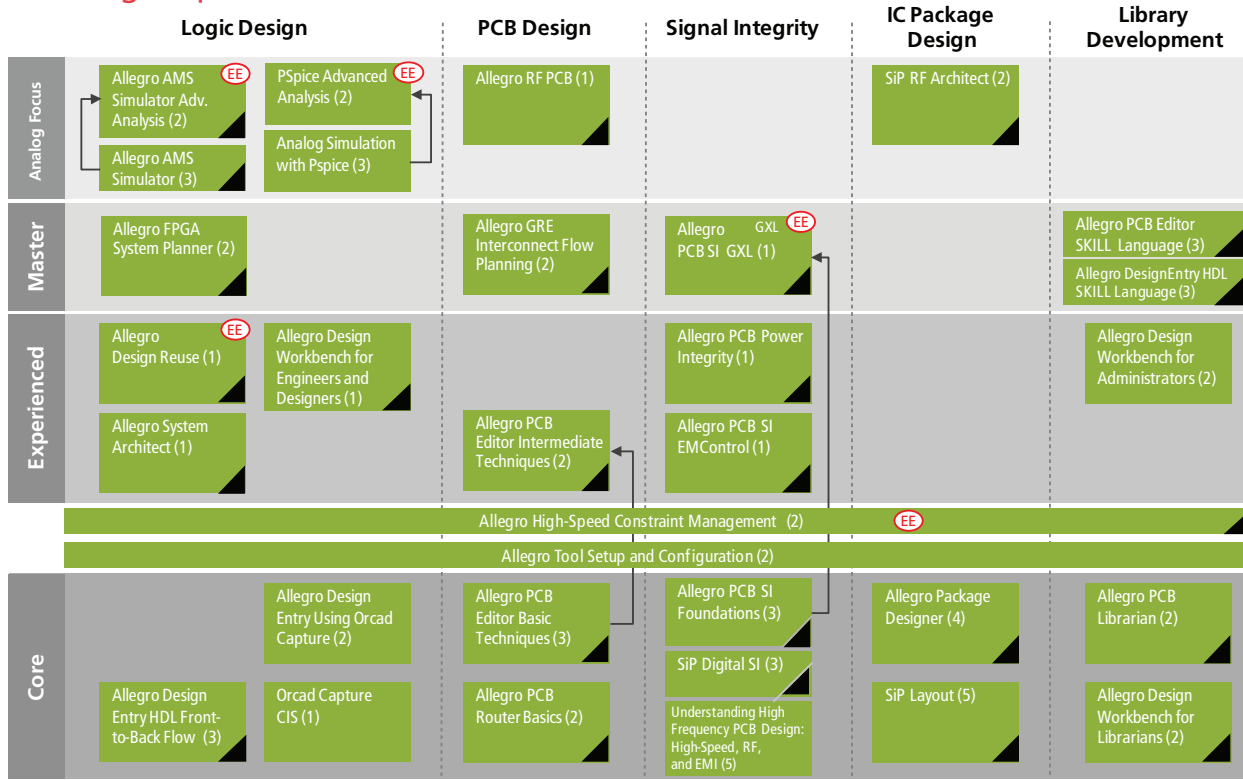
**Low Power:** In this course, you learn to verify low-power designs using Encounter Conformal Low Power.

**Encounter Conformal ECO:** In this course, you learn how to implement functional ECO analysis and generation, design netlist modification, clock domain synchronization, and semantics checks by using the Encounter Conformal ECO Designer tool.



# PCB and Package Design with Allegro Technology

## Learning Map



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## Course Descriptions

**Allegro High-Speed Constraint Management:** This course covers the application and verification of high-speed constraints across a design process. You learn to schedule nets, control impedance on nets, control the propagation delay from drivers to receivers, and match the propagation delay of driver and receiver pairs.

**Allegro Tool Setup and Configuration:** This course teaches you how to create a customized setup for many Allegro® tools that can be applied to a single user or across an entire company site. This tool setup course makes it easier for you to use the Allegro tools, to get new designs started, and to establish a standard environment that maximizes productivity.

### Logic Design

**Allegro Design Entry HDL Front-to-Back Flow:** This course teaches you how to create board-level schematic designs and demonstrates the integration between Design Entry HDL and other tools in the design flow, including the PCB Editor.

**Allegro Design Entry using OrCAD® Capture/OrCAD CIS:** This course covers front-end design processes such as setting up design templates, creating a netlist for board layout, and part management. The CIS class covers the CIS database, adding parts to the schematic, and modifying part properties.

**Allegro System Architect:** The course introduces you to a new paradigm in design entry, making use of a spreadsheet- or table-based System Connectivity Manager tool.

**Allegro Design Reuse:** Design reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse.

**Allegro Design Workbench for Engineers and Designers:** This course shows you how to create a new project, search and add parts to your schematic using the component browser, take the design to layout, and backannotate.

**Allegro FPGA System Planner:** This course shows you how to define your FPGA system and synthesize the connections in your design. You generate a schematic and PCB Editor database so the FPGA I/O assignments can be optimized in the board environment.

**Allegro AMS Simulator:** This three-day course starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the various simulations available in the Allegro AMS Simulator product.

**Allegro AMS Simulator Advanced Analysis:** In this course, you configure and run advanced analyses, including sensitivity, Monte Carlo, stress, and worst case. This course uses the Design Entry HDL schematic entry tool.

**Analog Simulation with PSpice:** This three-day course starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the various simulations available in the Allegro AMS Simulator product.

**PSpice Advanced Analysis:** In this course, you configure and run advanced analyses, including, Monte Carlo, stress, sensitivity, and worst case. This course uses the OrCAD Capture schematic entry tool.

## PCB Design

**Allegro PCB Editor Basic Techniques:** This course covers all the necessary steps for designing a PCB: from loading logic and netlist data, through producing manufacturing/NC output. This course is a prerequisite to the Allegro PCB Editor Intermediate Techniques course.

**Allegro PCB Editor Intermediate Techniques:** This course gives you a deeper understanding of the software and presents features and tips. In the task-oriented labs, you use a combination of interactive and automatic tools. You should attend the Allegro PCB Editor Basic Techniques course before attending this course, or have the equivalent work experience.

**Allegro PCB Router Basics:** This course teaches you how to use the Allegro PCB Router and interactive wire editing tools.

**Allegro RF PCB:** In this course, you learn about various RF PCB front-to-back flows.

**Allegro GRE Interconnect Flowplanning:** The Global Route Environment (GRE) provides the technology and methodology to capture as well as adhere to a designer's intent. In this course, you apply this technology and methodology to convert your design intent into the final board design.

## Signal Integrity

**Allegro PCB SI Foundations:** This course teaches you how to use the Allegro PCB SI tool to develop and drive design rules for high-speed designs. A design flow implementing a DDR2 memory interface on a PCB is presented.

**SiP Digital SI:** In this course, you will use the SiP Digital SI XL tool to analyze the high-speed nets in a multi-chip module. You will also use the Topology Editor to extract topologies from the design for analysis, as well as create your own topologies to explore design technology tradeoffs.

**Understanding High-Frequency PCB Design – High Speed, RF, and EMI:** Part 1 of this two-part course applies basic physical principles to develop an understanding of the issues of high-speed design, thereby ensuring a successful design for signal integrity. Part 2 builds on the principles and practices established in Part 1, extending them to develop techniques for design and test at frequencies above 1GHz for Gb/s serial transmission and for controlling the generation and propagation of EMI at the PCB level.

**Allegro PCB SI EMControl:** This course helps you to detect problems by enabling you to repeatedly check your design against selected sets of EMC rules chosen by a user who has expertise in EMC.

**Allegro PCB Power Integrity:** This course provides a coherent methodology for the design and fabrication of power distribution systems (PDS) in high-speed PCBs. Power distribution system design includes voltage regulator modules, decoupling capacitors, and power/ground planes.

**Allegro PCB SI GXL:** This course uses the Multi-Gigabit option of the Allegro PCB SI product to analyze high-speed channels using the advanced Channel Analysis simulator. You will characterize a channel and run high-capacity simulations with millions of bits using advanced IBIS-AMI models.

## IC Package Design

**SiP Layout:** This course takes you through a complete design flow of a system-in-package (SiP) design, from defining the module outline through placing components, defining a netlist, placement, routing, documentation, and manufacturing output. The course covers the complete design flow for a flip-chip and wire-bonded stacked die module using the Cadence SiP Digital Layout software.

**Allegro Package Designer:** This course discusses the Allegro Package Designer system. It covers the design and specifications for manufacturing single-chip modules for single-, double-, or multi-layered analog and digital packages.

## Library Development

**Allegro PCB Librarian:** In this course, you are introduced to the Library Explorer, the Part Developer, and PCB Editor. Next, you learn how to create a development and testing area for new Allegro Design Entry HDL (DE-HDL) and PCB Editor parts.

**Allegro Design Workbench for Librarians:** In this course, you will learn how to create a new project, new parts, new schematic models, and new footprint models. You will also be taken through an ECO flow to update an existing part.

**Allegro Design Workbench for Administrators:** This course is designed for users responsible for updating and maintaining the Allegro Design Workbench environment and databases.

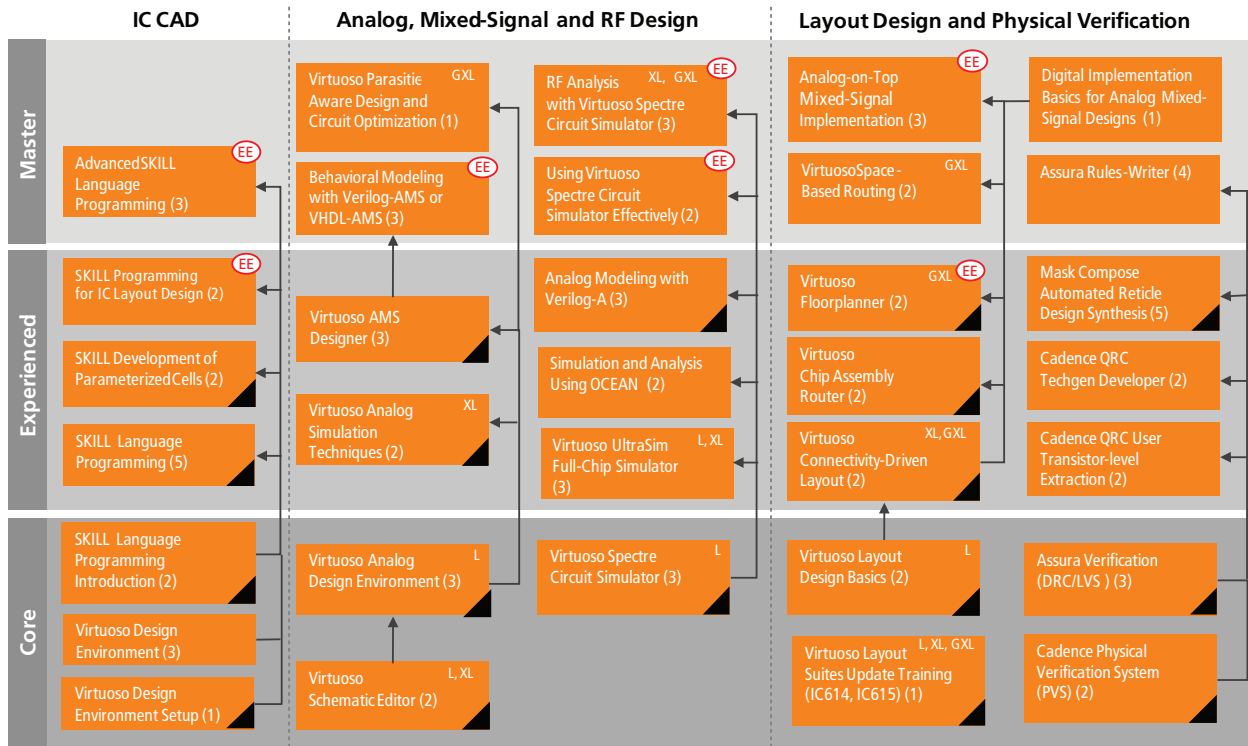
**Allegro PCB Editor SKILL Language:** This course provides the basic knowledge required to begin writing commands and functions to customize and extend the functionality of the base PCB Editor and Advanced Package Designer (APD) tool set.

**Allegro Design Entry HDL SKILL Language:** This course provides the basic knowledge required to begin writing useful commands and functions to customize and extend the functionality of the base Design Entry HDL tool set.

**SiP RF Architect:** In this course, you use a design flow between the Virtuoso design environment and the SiP Layout environment. You use this flow to create a single, system-level, circuit simulation-ready schematic for an RF/analog die, SiP substrate, and for packaged and embedded discrete devices.

# Custom Design with Virtuoso and DFM Technology

## Learning Map



▲ Also available as a self-paced course <sup>EE</sup> Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Not applicable if no legend. Some course titles may vary. Please refer to your regional catalog for exact titles and course datasheets. (#) Denotes number of days for instructor-led training. Several self-paced courses are only available in our [Online Training Collection](#)

## Course Descriptions

**Virtuoso Schematic Editor:** Learn how to create schematics, their corresponding symbols, and navigate a design hierarchy. Create design constraints using the Constraint Manager and the Circuit Prospector, and learn to use inherited connections.

**Virtuoso Analog Design Environment:** Learn how to simulate analog circuits in the ADE-L environment using Spectre® and APS Simulators. Use the ViVA XL Waveform Viewer and analyze simulation results. Modify the CDF for an instance. Perform device checking and run parametric sweeps. Use the Hierarchy Editor to switch between multiple design views. Use Virtuoso Power System to evaluate IR drop and electromigration.

**Virtuoso Analog Simulation Techniques:** Using the ADE-XL environment, learn to simulate multiple testbenches simultaneously using various assistants and workspaces. Perform multiple sweeps and corners analyses, parameterize your design, simulate to meet specs, perform Monte Carlo analysis, and create datasheets.

**Virtuoso Parasitic-Aware Design and Circuit Optimization:** Using the ADE-GXL environment, create parasitic-aware designs by estimating and extracting parasitics. Run feasibility analysis, create worst case corners, and employ optimization methods.

**Simulation and Analysis with OCEAN:** Explore how to use OCEAN to run analog/mixed-signal simulations and to manipulate your simulation results.

**Virtuoso Spectre Circuit Simulator:** Use Spectre Simulator from the command line to run complex simulations. Learn about Spectre-SPICE compatibility. Examine and run DC, transient, reliability, Monte Carlo, and small-signal analyses from the command line. Learn how to use the APS Option and Spectre MDL.

**Using Virtuoso Spectre Simulator Effectively:** Get an in-depth look at Spectre Simulator. Learn about DC and AC analysis algorithms and how they affect simulation. Learn how transient analysis simulates and how to evaluate DFT.

**RF Analysis with Virtuoso Spectre Circuit Simulator:** Learn about the Spectre RF Simulation Option. Set up, simulate, and analyze various RF designs in a receiver chain. Run PSS and QPSS analyses using the Shooting Newton and Harmonic Balance algorithms. Perform noise analysis, evaluate jitter, and learn about Envelope analysis.

**Virtuoso UltraSim Full-Chip Simulator:** Learn how to use this FastSPICE simulator to run large transistor-based simulations, including an extensive set of checking commands, power analyses, and IR drop and electromigration tests.

**Virtuoso AMS Designer:** Learn to run and debug large, complex mixed-signal/mixed-language simulations using Verilog, Verilog-A, Verilog-AMS, schematic views, Spectre, and SPICE design blocks in mixed configurations. Run AMS Designer from the command line and from the ADE GUI. Debug simulations using SimVision. Use the AMS Incisive flow for design verification. Create real-valued models using the wreal capability.

**Behavioral Modeling with Verilog-AMS or VHDL-AMS:** These courses provide an in-depth approach to writing realistic behavioral models of analog/mixed-signal design blocks and systems using either Verilog or VHDL languages.

**Analog Modeling with Verilog-A:** Use Virtuoso ADE and Spectre Simulator to simulate analog circuits using Verilog-A models. Use Verilog-A to model and design an analog-to-digital converter and parts of a PLL.

**Analog Modeling and Simulation with SPICE:** Get a better understanding of device modeling, deep-submicron technology, and the operation of a SPICE circuit simulator. Learn about structural and behavioral modeling differences, simulation controls available to the user, and steady-state analysis.

## Physical Design

**Analog-on-Top Mixed-Signal Implementation:** This two-day course focuses on the interoperability between digital (Encounter) and analog (Virtuoso) environments, which share a common database. Set up the environment and drive the flow to create and insert a digital block into an analog custom IC design. The first day is the optional Digital Implementation Basics for AMS Designs course.

**Virtuoso Layout Design Basics:** Learn the basic techniques for working with Virtuoso Layout Suite L. Create and edit cell-level designs, and create and place instances to build hierarchy for custom physical designs.

**Virtuoso Connectivity-Driven Layout:** Use example IC layouts to explore schematic-driven layout techniques. Virtuoso Layout Suite XL provides many features and automation improvements to assist you.

**Virtuoso Space-Based Router:** Space-Based Router runs within Virtuoso Layout Suite GXL. Learn how to quickly capture and manage block- and chip-level routing solutions using the Process Rules Editor as well as customized Tcl scripts.

**Virtuoso Floorplanner:** Use the floorplanner to calculate the area needed for the top-level boundary and blocks. Place the I/O pads, generate and place the top-level blocks, and complete a top-level floorplan.

**Virtuoso Physical Design Update:** Learn about the new layout design features, GUI, and use models of the 6.1 platform. This course is designed for those familiar with previous releases (such as 5.1.4.1) who are moving to the new platform; it does not cover migration steps.

## Infrastructure

**Virtuoso Design Environment Setup:** Learn to install the software, manage licenses, and troubleshoot file-locking issues.

**Virtuoso Design Environment:** This course covers administration, such as installing the software, managing licenses, using PDKs, customizing the environment, troubleshooting file-locking issues, and using SKILL commands.

**SKILL Language Programming:** This course provides the comprehensive foundation, concepts, and sample programs to build SKILL programs.

**SKILL Language Programming Introduction:** Get the basic SKILL language foundation to write and debug SKILL procedures in just two days.

**SKILL Programming for IC Layout Design:** Learn how to use SKILL programs to automate layout tasks.

**SKILL Development of Parameterized Cells:** Use SKILL to develop Pcells, the building blocks needed to leverage the connectivity-driven design environment for productivity gains.

**Advanced SKILL Language Programming:** This course focuses on the lexical scoping and object-oriented extensions to the SKILL language, known as SKILL++.

## Verification

**Cadence Physical Verification System:** Learn practical methods of running and debugging DRC, ERC, and LVS. Use the powerful PVS debugging environment to locate errors and fix real problems quickly.

**Assura Rules Writer:** Learn how to write and optimize rules for Assura® physical verification.

**Cadence Assura Verification:** Learn about all aspects of using Assura tools for design rule checks, short location, and layout versus schematic checks.

**Cadence QRC User Transistor-Level Extraction:** This course covers Cadence QRC transistor-level parasitic extraction for analog and full-custom circuits.

**Cadence QRC Techgen Developer:** Get an overview of parasitic extraction, and then use existing RCX or QX tech files to create a tech file for the new QRC extractor.

**MaskCompose Automated Reticle Design Synthesis:** Learn how to define a flow and process, build a reticle layout, produce documentation, generate a wafer layout, and use techniques that accelerate the DFM process.

## Digital Implementation

**Digital Implementation Basics for Analog/Mixed-Signal Designs:** Learn to use Encounter Digital Implementation System to implement your AMS designs. Explore floorplanning, placement, power planning, clock-tree synthesis, timing optimization, and detail routing. This course is typically offered as the optional first day of the AoT Mixed-Signal Implementation course for new Encounter users.

# Training Locations

## North America

### Arizona

Cadence Design Systems, Inc.  
1620 W. Fountainhead Pkwy, Suite 308  
Tempe, AZ 85282  
Location Tel: (480) 413-9550  
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### California

Cadence Design Systems, Inc.  
2655 Seely Avenue, Bldg. 6  
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### Texas

Cadence Design Systems, Inc.  
12515-7 Research Boulevard, Suite 250  
Austin, TX 78759  
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### Massachusetts

Cadence Design Systems, Inc.  
270 Billerica Road  
Chelmsford, MA 01824  
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### Ottawa, ON, Canada

Cadence Design Systems LTD  
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