



CADENCE AND CELESTIAL SEMICONDUCTOR

Cadence Encounter Platform Helps Celestial Develop High-Speed Multimedia IC Based on 0.13 μ m Process

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John A.Thodiyil, Technical Director, Celestial Semiconductor Inc. (Beijing)

CORPORATE PROFILE

- Celestial Semiconductor develops integrated circuits for decoding AVS, MPEG2, H.264, and other standards

DESIGN CHALLENGES

- Convert to a 0.13 μ m process while increasing the frequency to 220MHz
- Minimize the impact of IR drop and signal integrity
- Tape out the chip in a very tight project schedule

CADENCE SOLUTION

- Cadence® Encounter® digital IC design platform

CADENCE PRODUCTS AND SERVICES

- SoC Encounter™ RTL-to-GDSII System
- VoltageStorm® Power Analysis
- Encounter Timing System
- Cadence Services

CHALLENGES IN 0.13 μ m DESIGN

Celestial Semiconductor Inc. (Beijing) develops integrated circuits for decoding AVS, MPEG2, H.264, and other standards. In the past two years, Celestial has developed the AVS decoding chip based on China standards as well as the MPEG2 decoding chip based on international standards, which have 5M+ gates and 160MHz in frequency. Both of these chips have taped out.

The MPEG2 decoding chip project in particular faced a new set of challenges, such as higher technical requirements and a much tighter schedule. To lower the cost, Celestial decided to convert its 0.18 μ m process to a 0.13 μ m process, and then increased the frequency to 220MHz. With the Celestial back-end team’s limited experience in 0.13 μ m process design, the inherent complexity of completing a 220MHz design by embedded application

CPU, and a narrow time-to-market window, the Celestial team simply could not afford a long learning curve or multiple iterations.

In 0.13 μ m designs and below, both IR drop and signal integrity (SI) have great impact on the entire design process. Even the smallest default will cause chip failure. To avoid re-spins, the Celestial engineering team needed a wire-centric methodology to account for the effects of interconnect across the entire chip—from the very beginning of the design cycle—complete with power and timing analysis and SI prevention and fixing capabilities.

MANAGING IR DROP

Cadence VoltageStorm Power Analysis, a key technology in the Cadence Encounter digital IC design platform, delivers leading-edge power and power rail analysis. By adopting VoltageStorm technology, Celestial designers benefited from accurate instance-based power calculation and IR drop impact on the IC.

This data also played an important role in the design of power rail routing and the number of power I/Os. VoltageStorm technology helped Celestial keep the total IR drop to less than 5%.

ADDRESSING SI ISSUES

For 0.13 μ m technology, crosstalk analysis is crucial. Cadence Encounter Timing System offers a consistent, integrated static timing analysis (STA) environment for place-and-route optimization and signoff verification. It combines the CeltIC® Nanometer Delay Calculator's production-proven SI analysis capabilities with Cadence technologies for timing and power analysis, delay calculation, advanced modeling, and global timing debug. Celestial adopted Encounter Timing System to analyze both the impact of crosstalk on timing and of glitch on logic. Using Encounter Timing System enabled the Celestial design team to avoid uncontrollable errors in post-routing analysis.

ACHIEVING TIMING CLOSURE IN 220MHZ MODE

As Celestial shifted to the 0.13 μ m process, it became more difficult to achieve the 220MHz design. On this front, the Cadence SoC Encounter RTL-to-GDSII System played an important role. By optimizing the interconnect and setting up regions in key paths, the SoC Encounter system made it possible for the Celestial team to achieve timing closure.

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