

NEC Electronics Corp. saw significant **“Design Cycle Time Reduction and Performance Improvement with optimized Leakage Power”** on 2 benchmarks using Encounter® RTL Compiler

NEC
NEC Electronics Corporation

NEC Electronics Problem

- **No tight correlation** between logical synthesis and layout
- **Difficult to optimize** leakage power to meet target performance
- **Very complex synthesis flow** for Low Power (Multi-Vt, Multi Supply Voltage) and Datapath
 - Long synthesis turnaround time
 - Hierarchical design flow



Cadence Solution

- **Less iteration** between front-end and back-end design with “Design with Physical” solution
- **10~20% leakage power reduction** with better performance than conventional tool
- **1 Pass (Top Down) synthesis flow**
 - for Low Power
 - Multi-Vt Leakage optimization
 - Multi Supply Voltage
 - for Datapath
 - No more MCL and DW

Good trade-off between performance and leakage power !!

- 10~20% leakage power reduction with better performance

Significant improved synthesis turnaround time !!

- From 2~3 days work to 0.5 days