



Utilizing volume diagnostics data to improve yield

Dale Meehl and Tom Jackson, Cadence Design Systems

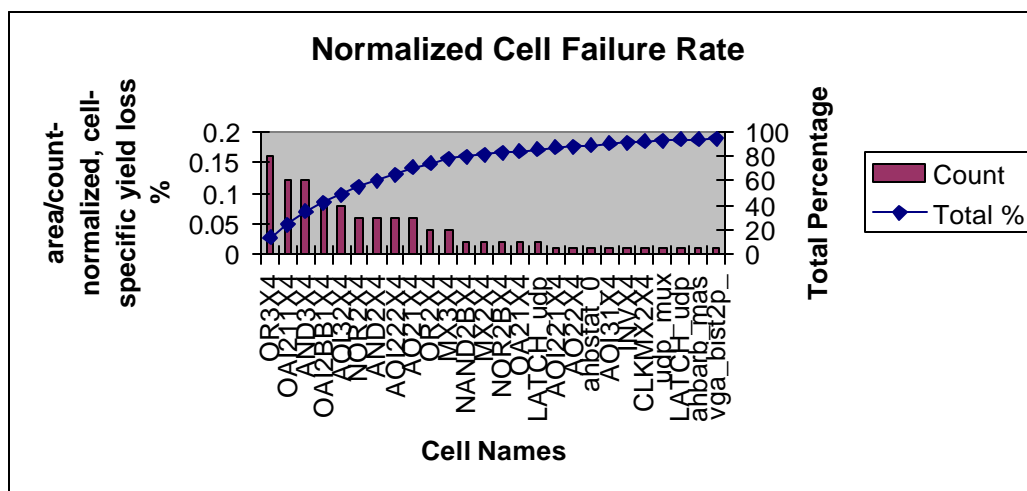
Volume diagnostics

Volume diagnostics analyzes results from wafer sort or final test utilizing failsets from automatic test equipment (ATE). These failsets include both input test patterns and measured miscompares on both scan and output pins. Typically, a batch diagnostics engine runs on parallel compute resources and will analyze hundreds, if not thousands, of failsets for a single device type. The diagnostics engines run fast and will accurately rate a set of faults for their correlation to each failset. In most cases, if the sample of failsets from a wafer lot is large enough, and if the failures are due to systemic issues, then the results would be accurate and show a high degree of commonality among failures. Potential design and/or process fixes would then have a very high probability of being successful.

In the example described in this article, a semiconductor company utilized Cadence Encounter Diagnostics software to analyze results from their wafer electrical test (WET) process for a large nanometer device and found several common circuit elements involved in a substantial number of failing devices. This information was extremely helpful in their yield enhancement efforts. The failure sample size was hand picked after some basic human analysis and consisted of more than 400 failsets. After Encounter Diagnostics generated all callout data, several types of analysis were run against the data to find commonality among device failures.

Cell summary report

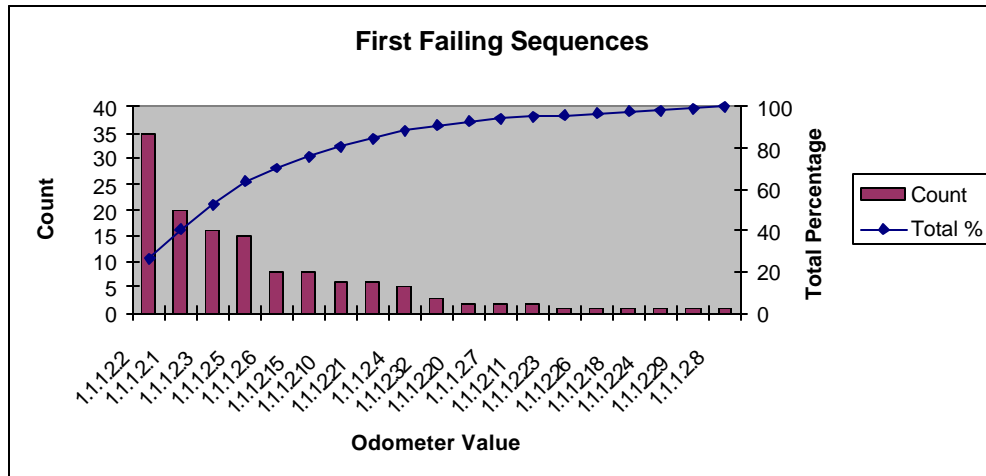
This report shows yield loss attributed to a specific cell type. There are several methods to normalize cell data including by die area, transistor count, and so on. In the specific case shown, normalization is by die area in cm^2 and instance count. The chart displays the most common failing cells within the wafer lots analyzed by Encounter Diagnostics.



Data from cell summary reports could direct design engineers to examine layout and placement locations of adjacent cells for the top failing cell types to ascertain

Failing test sequence report

This report highlights the failing test sequence that occurs most often.



This information, used in conjunction with other data and reports, would help guide yield enhancement efforts; engineers could sequence this test to the front of the test suite to optimize testing efforts.

Precision yield diagnostics

Volume diagnostics provides highly accurate samples of defect categories from its reports, which can pass directly to precision yield diagnostics (PYD). PYD is a methodology that provides more advanced analysis to determine the specific root cause of the most subtle nanometer design-process interaction defects. PYD normally deploys to precisely locate the root cause defects in a given silicon die. In most cases, PYD can trace failures down to a particular interconnect wire. This information, in turn, drives various failure analysis (FA) processes to aid in both non-destructive and destructive exploration to point to the exact failure site/structure on a single die.

Conclusions

Ramping yield in a nanometer fab is essential, and today's semiconductor companies are actively employing new techniques such as volume diagnostics in an attempt to locate and take action on faults caused by systemic design-process interactions. This paper shows a real-world example of this process and how design and fab personnel can use the information provided by volume diagnostics to improve yield.

Authors

Dale Meehl is a senior member of the consulting staff in the Cadence Encounter Test group. Prior to Cadence, Dale worked in EDA solutions for IBM Microelectronics. Dale has a B.S. in Electrical Engineering from Clarkson University.

Tom Jackson is currently a marketing director for the Cadence Encounter Test group and is responsible for diagnostics products. Tom has almost 20 years of EDA experience and began his career as a test engineer working on hardware accelerators. Tom has also held various positions in field applications and product marketing in the areas of design for test, formal verification, and yield management.