

COLLABORATIONS

AUGUST 2007



Low-Power Design: It Takes Design Chain Collaboration

Welcome to the summer edition of the Cadence® *Collaborations Newsletter*. Our goal is to keep you updated on our latest partner activities to maintain an active and well-informed Cadence design chain. This edition focuses on low power and highlights our work with foundry, IP, EDA, and manufacturing partners to deliver leading-edge, power-aware design methodologies that remove the barriers to low-power design innovation.

Low-power design is driving the semiconductor, EDA, and electronics industries. As CMOS process is revealing its limitations, power consumption has become a huge issue. As such, companies are trying innovative approaches: new products and flows, new processes, *and* new design techniques. But incorporating the most advanced low-power techniques can increase design complexity and may introduce risk that destabilizes a team's existing flow. And since many of these power-reduction techniques are so new, conventional technologies lack an automated methodology for implementing them. The result is a costly, ad hoc approach to low-power design.

To ensure customer success, innovative low-power design solutions must be

- 1) holistic and automated;
- 2) defined by user/vendor collaboration;
- and 3) refined

through user-driven adoption. Any major industry challenge like this requires industry-wide collaboration.

Cadence started this collaboration with Applied Materials, ARM, Artisan, and TSMC back in 2003 under a partnership called the Silicon Design Chain (SDC). The SDC developed many low-power test chips. In each of these projects, we experimented with multi-supply voltage, dynamic voltage frequency scaling, power shut-off, test, and formal verification. Our work in low power revealed two main challenges to introducing such advanced techniques: high risk of failure and low productivity. Our jointly developed reference flows automated portions of the design and verification process, but manual work was still required, compromising productivity and time to market.

Recognizing the urgent need for automation, Cadence developed a comprehensive approach to automating low-power design, as well as the Common Power Format (CPF). CPF captures all power-specific design, constraint, and functionality requirements in a single file to enable holistic automation of advanced low-power techniques.

In May 2006, Cadence formed the Power Forward Initiative to create an ecosystem

of support and refine the format. The initiative was announced with 10 founding members (Applied Materials, ARM, Cadence, TSMC, and 6 users), and within 6 months reached a 20-member milestone, adding IP and EDA partners. During this time, we collected 500+ member inputs, incorporated them in CPF, and contributed the format to Si2. Si2's Low-Power Coalition then approved it as a standard in March 2007 and will continue to refine CPF as needed in a user-managed, user-driven, and IP-safe process.

Ongoing collaboration on low-power methodologies—and our consistent progress therewith—has made it possible for mutual customers to adopt new process geometries and incorporate advanced power-reduction techniques. With a holistic approach to power management, mutual customers can focus their time and resources on what matters most—innovation.

Thanks to many of you who've helped to make a real difference in moving the industry forward on low-power design.

Jan Willis
Senior Vice President, Industry Alliances
Cadence Design Systems

Annual Design Chain Partner Event

Save the date for the sixth annual Design Chain Partner Event, to be held on Wednesday, October 23, 2007 at the Corinthian Events Center in San Jose, CA. Hosted by the Cadence® Industry Alliances team, the event recognizes partners across the design chain and offers them a chance to meet with Cadence executives and experts to learn more about our strategy. Join other leading foundry, IP, ASIC, EDA, and verification partners to share your expertise and hear viewpoints on the future of low-power design.

More than 125 people attended last year's Design Chain Partner Event in November, which focused on the hottest topic: low power. "The low-power theme really resonates with partners," said Jan Willis, Cadence Senior Vice President of Industry Alliances. Keynote speaker Aurangzeb Khan, Cadence Corporate Vice President

and General Manager of Design Foundries, shared his team's low-power work on ARM 1136 and 1176 designs. During a panel discussion, Chi-Ping Hsu, Cadence Corporate Vice President, provided more details on CPF to reinforce that it's real and on its way to becoming an industry standard, despite the initial political wrangling.

"We also introduced the Partner Awards program in 2006, and that attracted a number of executives to attend," said Willis, who gave out awards with Cadence CEO Mike Fister in each of four categories recognizing operational excellence:

- Relationship management – ARM received the award for the CEO and senior executive-level sponsorship of the alliance and dedicated relationship-management staff

- Joint marketing – ARC was the award recipient for their participation and sponsorship of multiple joint marketing and business development activities
- Whole product engineering – Fujitsu received the award for their resource commitment and timeliness of support of Cadence products
- Sales support – TSMC received the award for having achieved the highest number of customer references

We invite you to attend the next Design Chain Partner Event in October. It's an excellent opportunity for you to meet Cadence executives, network with other experts and industry partners, and learn more about the latest in low-power solutions.



ARM's Joe Convey accepts the Relationship Management Award



ARC's Karl Auker accepts the Joint Marketing Award

Power Forward Initiative News: Growing the Ecosystem for Low-Power Design

Just one year ago, 10 companies launched the Power Forward Initiative (PFI) to drive advanced low-power design. Since that time, 13 more companies joined PFI, including representatives from the EDA, IP, foundry, and manufacturing equipment communities. Recognizing the urgent need for an automated, power-aware design infrastructure, these industry leaders participated in the rapid evolution of the Common Power Format (CPF), enabling its early contribution to Si2 and its subsequent ratification as an Si2 standard. CPF 1.0 is now available to everyone as a standard, at no cost, from Si2 at www.si2.org.

The Power Forward Initiative has made significant progress in delivering advanced low-power design capabilities and growing a broad ecosystem to support advanced low-power design using Si2's CPF 1.0 standard format. A number of the PFI advisory members are executing proof-point projects to bolster support for the Common Power Format (CPF) and create holistic, scalable low-power design flows. Advisory members include AMAT, AMD, ARC, ARM, ATI, Azuro, Cadence, Calypto, Denali, Freescale, Fujitsu, Globetech, Improv, MIPS, NEC, NXP, Sequence, Tensilica, TSMC, UMC, Virage, and Vivace.

ECOSYSTEM SUPPORT

Foundries

In late March, TSMC announced availability of their CPF-enabled 65nm library. In early April, UMC joined the Power Forward Initiative with the intent of supporting a complete low-power design flow based on CPF. Soon after, the Common Platform Manufacturing collaboration among IBM, Chartered, and Samsung announced the availability of a 65nm CPF-based low-power reference flow.

IP vendors

At the Design Automation and Test (DATE) Conference in April, ARC announced a CPF-enabled low-power reference methodology for their 700 D configurable processor. The 700 D CPF-enabled flow will be available later this year and will incorporate Virage libraries and memories,

which are currently undergoing final testing and will be available broadly later this year.

EDA vendors

In April, Calypto announced support for CPF in their PowerPro CG clock gating optimization tool. In an interview published in *EETimes*, Devadas Varma from Calypto said, "So far we've been driven primarily by customer requests and what tools are available to support a given format. We are not supporting other low-power formats at this point." Also in April, EDA vendors Atrenta and Sequence both communicated their plans at the DATE conference to support CPF in their products by the second half of 2007.

PROOF-POINT PROGRESS

Each of the founding PFI members collaborates with Cadence to complete a proof-point project, with Cadence providing technical support. A proof-point project exercises CPF-enabled Cadence® low-power design technologies to validate that the format works holistically. With focused scope (from one to three months), each project consists of a mainstream design as small or complex as required according to the project needs. Proof-point projects may include using CPF-based solutions to explore alternative low-power techniques, such as multi-supply voltage (MSV), state-retention power gating (SRPG), power shut-off (PSO), and dynamic voltage frequency scaling (DVFS).

These projects ensure the CPF-based low-power flow meets or exceeds the partner's design requirements. Proof-point projects do not benchmark Cadence products, nor are they intended to validate the low-power savings provided by using Cadence technologies with CPF. Rather, they validate that the Cadence Low-Power Solution is holistic, scalable, and productive. PFI member companies provide feedback to Cadence and Si2's Low Power Coalition, helping to improve and refine CPF and the integration of the low-power design flow. Results of proof-point projects may then be used to advance the holistic solution for Cadence and PFI members, and to offer the greater electronics industry a

comprehensive, proven approach to incorporating advanced low-power design techniques and differentiating their products.

LOW-POWER EVENTS

SEMICON SHANGHAI 2007

In March, the Fabless Semiconductor Association hosted a low-power event co-sponsored by Cadence at SEMICON in Shanghai. Power Forward Initiative members Felix Fei from ARM, Jan Willis from Cadence, and YC Wu from TSMC were joined by Nianfeng Li from Verisilicon, a prominent Chinese design house, and Frank Childers from Si2 to present low-power design experiences and progress on the adoption of CPF. The event concluded with a panel discussion moderated by Mike Clendenin, *EETimes* Asia bureau chief. The audience in China was eager to hear the latest progress on the most advanced low-power design solutions in use today.

DAC 2007

There was a "Productivity Improvement and Risk Reduction in Low-Power Design" Low-Power Lunch Panel and a Si2 organized low power workshop at DAC. More details on these events are in the DAC "Co-Sponsored Events, Workshops, and Panels" article on page 7.

DATE 2007

In April, members of the Power Forward Initiative participated in a panel discussion at the DATE conference. Colin Holehouse from ARC, Vic Kulkarni from Sequence, Dave Gross from Freescale, and Steve Schulz from Si2 shared their successes with CPF and discussed the progress made toward industry-wide deployment. Pankaj Mayor from Cadence moderated the panel.

WHAT YOU CAN DO

Users are demanding low-power solutions that work TODAY; their suppliers are responding with support for CPF-based solutions. We encourage all members of the OpenChoice IP and Connections® programs to become part of the rapidly growing ecosystem supporting Si2's Common Power Format.

TSMC Libraries Support CPF-Enabled Low-Power Design Flow

George Kuo, TSMC Foundry Program

Cadence and TSMC have been collaborating through the Power Forward Initiative to enable more efficient utilization of low-power design techniques at 65nm and below. As a result of these ongoing efforts, the two companies recently announced the availability of 65nm low-power libraries from TSMC that support the Si2 Common Power Format (CPF). CPF enables low-power design intent to move seamlessly through the design, verification, and implementation of a chip. It automates advanced low-power design techniques such as clock gating, power shut-off (PSO), multi-supply multi-voltage (MSMV), and dynamic voltage frequency scaling (DVFS). It also offers verification coverage of non-logic low-power features. Because CPF eliminates manual intervention and manages the design flow more efficiently, it reduces the risk of errors and delivers faster turnaround time for power analysis and timing closure.

To validate the CPF-enabled flow, TSMC engineers first ensured that the 65nm libraries contain all components required to support the flow's advanced low-power design techniques. Cadence then ensured that the 65nm libraries work seamlessly with Cadence® Low-Power Solution components. These technology components integrate logic design, verification, and implementation technologies with CPF, which specifies power-saving techniques early in the design process—enabling designers to share and reuse low-power intelligence. It also helps design teams achieve superior tradeoff among timing, power, and area requirements.

TSMC's validation of CPF as the industry's first complete, production-worthy low-power design flow is a key endorsement from a major foundry. CPF support in TSMC libraries enhances the design experience for mutual customers, who now have a guaranteed methodology for

low-power design success. Such seamless integration of TSMC libraries, Cadence low-power technologies, and CPF means that customers benefit from faster design and debug cycles. Most importantly, they can focus their engineering resources on enhancing product performance and functionality, not the implementation details of a low-power flow.

Cadence and TSMC have worked closely on low-power techniques since 2003. The CPF-enabled design flow that we have proven through this collaborative work delivers the productivity necessary to accelerate the adoption of advanced low-power design techniques. When partners truly focus on the customer's design challenges, it's possible to find new, holistic solutions that combine the best offering of both partners to enable differentiated products.

OpenChoice IP Program Update

Pat Dutrow, OpenChoice Program

WHAT'S NEW WITH OPEN-CHOICE?

For those not familiar with the OpenChoice IP program, simply put, it is a collaborative partnership program designed to make IP integration easy for mutual customers. By partnering with market-segment-leading IP providers, the OpenChoice program enables customers to easily integrate complex third-party IP blocks into their SoCs. Our partner IP portfolio covers the full gamut of digital, analog, soft, hard, and verification IP, giving our customers the greatest choice and flexibility for selecting the best IP suitable for their particular applications. The program now

has 40 members, who you can learn more about at www.cadence.com/partners/ip_program. Recently, we've added new team members to the OpenChoice staff, each filling critical roles to help us execute on our program strategy. These new team members are responsible for three areas:

1. managing relationships with and among OpenChoice program members
2. helping program members leverage the extensive Cadence sales channel and drive wider exposure to mutual customers

3. helping identify and test IP that can be made compatible with Cadence the methodology kits focused on vertical segments

CALL TO ACTION

Any time you advocate your joint solution through a public presentation, a sales call, or a visit to a customer with a Cadence representative, please talk to your OpenChoice alliance manager about it. As we work together, we can collaboratively meet our customer IP needs and further enhance our mutually beneficial relationships.

Fifteen Years of Cadence Connections Progress

Ken Nakano, Connections Program

The Cadence® Connections® program celebrates its 15th anniversary this year, and what a groundbreaking trip it's been. The first such effort of its kind, the Connections mission of encouraging interoperability in the name of customer success has now become standard procedure in the industry. And 15 years later, the Connections mission is still leading the way. The program continues to expand, as does our commitment to ensure that mutual customers have the best combination of compatible, innovative technologies to meet their design goals.

From accelerated layout to yield management, 137 Connections members provide combined flows from 25 design-task categories, giving EDA users a vast expanse of choices. And choice is crucial to customer success because no two electronic design projects are alike. The ability to combine the best of what the

EDA industry has to offer, in ways that match specific design-project requirements, has shown itself again and again to be a critical success factor.

Cadence conceived of the Connections program in 1991, and by 1992 it was in full swing. In its first 15 years, the program has grown to 137 members – the largest and most encompassing of similar EDA programs. With the Connections program, members choose from three levels of connecting with Cadence tools: *encapsulation*, *interfacing*, and *integration*. Encapsulation permits a member tool to launch from within the Cadence environment. Interfacing supports batch exchange of data. And, integration offers real-time, tool-to-tool interaction and communication.

Cadence makes it easy for third-party EDA vendors to take part in the Connections program. The process starts with an

online application available on the Connections website www.cadence.com/partners/connections. Aspiring members must have products already in the market and customer requests for integration with Cadence technologies. Upon joining, members receive Cadence software at minimal cost and take part in a comprehensive process for enabling the integration of their tools with those of Cadence.

Connections members span the design spectrum and support the entire flow, from ESL for architectural exploration through development and manufacturing. Verification tool, PCB software, and custom IC tool vendors make up about three-fourths of Connections-enabled flows, evenly split among the disciplines. The remaining is a mix of ESL tools, digital IC physical design tools, physical verification tools, and DFM software.

DAC 2007 REPORT

PARTNER TECH TALKS

This year's Design Automation Conference (DAC) featured an open presentation theater where Cadence® and partner technologists gave dynamic Tech Talks. Partner presentations comprised 17 of the 26 half-hour Tech Talks, which addressed a wide range of design topics.

Tech Talks are an excellent way for our partners to showcase their technologies as well their collaboration with Cadence.

Partner	Tech Talk Title
HDL Design House Predrag Markovic, CEO	Addressing Complex SoC Verification Challenges While Lowering Costs and Increasing Quality
Rambus Prakash Rashinkar, Director of Engineering	Integrating Design IP and Verification IP to Ensure Quality and Enhance Productivity
IBM Keith Barkley, Sr. Software Engineer, High-Performance Processor Design	High-Performance Routing and DFM for Next-Generation Custom Processor Design
STMicroelectronics Laurent Ducousso, IP Verification Manager	SystemC TLM for Verification of Complex IP
Optimal Dr. Marc E. Kowalski, Sr. Application Engineer & Technical Marketing Manager	Stable, Clean, and Accurate Power from PCB to Package to Chip
RF Micro Devices Cory Ellinger, Sr. Engineer, Corporate CAD, Digital Design	Encounter Low-Power Flow Adoption
TSMC LC Lu, Ph.D., Deputy Director at DTP	Low Power and TSMC Reference Flow
Denali Brian Gardner, VP of IP Products	Holistic Power Control in Memory Subsystems
Analog Devices Kelly Larson, Verification Manager, Austin Design Center	Using Class Libraries for Efficient Testbench Reuse in SystemVerilog
Verilab David Robinson, Verification Consultant and Partner	An Introduction to Aspect-Oriented Verification
ARC Colin Holehouse, Chief Engineer	Active Power Management Design for ARC Microprocessor Systems
Optimal An-Yu Kuo, Chief Technical Officer	Chip Thermal and Power Management Within the Packaging Environment
TSMC Steven Chen, Department Manager, Process Design Kits	Advanced PDK
Lightspeed Logic Albert Rich, Principal Engineer	Reconfigurable Logic CPF Flow for Imaging, DTV, and Basestation Applications
Silicon Hive Ir. Menno M. Lindwer, PDEng, Director of Product Management, Tools	Building Systems using Silicon Hive Processors
MOSAID Graham Allan, Director of Marketing and Jody Defazio, Director of Engineering for Semiconductor IP	Using Configurable Hard IP to Implement High-Performance Interfaces to External DDR SDRAM



IBM's Keith Barkley gives a Tech Talk on high-performance routing and DFM

CO-SPONSORED EVENTS, WORKSHOPS, AND PANELS

At the Cadence-ARM Wireless Technical User Group Meeting, Dr. John Goodenough, ARM Director of Design Technology, and Amjad Qureshi, Cadence Engineering Director of Wireless SoC Architecture, presented examples of the collaboration between ARM and Cadence that's helping wireless designers improve their productivity with jointly developed reference flows.

The topic was "Optimizing the Path into ASIC for First-Time-Right Silicon" at the Cadence-IBM Seminar. Breakfast attendees heard about an optimized front-end design methodology to accelerate their ASIC design success. IBM presented their ASIC roadmap for 65nm and 45nm technologies. Presenters were David Lackey of IBM (on IBM ASIC solutions), Tom Jackson of Cadence (on front-end design for IBM ASICs), and Tony Niolu and Rich Powlowsky of Cadence (on engaging with IBM/Cadence).

Cadence and Doulos held a lunchtime Solutions Workshop on "Adopting a Plan-to-Closure Methodology Across Design Teams and Verification Teams." Jonathan Bromley of Doulos discussed "Constructing SystemVerilog Universal Verification Components (UVCs)" and

Hamilton Carter of Cadence presented on "Plan- and Metric-Driven Verification." Attendees got the details on a methodology for creating an executable verification plan to block-, chip-, and system-level verification closure.

There was also Lunch Panel titled "SystemVerilog Design with Verification: Oil and Water Can Mix." The panel addressed how SystemVerilog is enabling

easy adoption of Design with Verification, a new Cadence environment where logic designers can leverage formal analysis and sophisticated testbenches at the block level, and how it links to full-chip verification. Panelists included Kelly Larson of Analog Devices, Jon Michelson of Verification Central, Tim Plyant of Cadence, Ambar Sarkar of Paradigm Works, and Noumaan Shah of Emulex.

The topic was "Productivity Improvement and Risk Reduction in Low-Power Design" at the much-anticipated Low-Power Lunch Panel. Panelists addressed the recent activity at several companies developing new approaches to help specify, manage, and communicate power-related information and constraints consistently throughout the design flow. Panelists included: Chris Rowen, Founder and CEO, Tensilica; Nader Vasseggi, Sr. Director and General Manager, Cisco; Dr. Devadas Varma, Chairman and Co-Founder, Calypto; Eric Filseth, Vice President of Product Marketing, Cadence; and Dr. LC Lu, Deputy Director of the Design Methodology Program, TSMC.

In a successful workshop organized by Si2, attendees learned more about standards for low-power design intent. Presenters and their topics were: Gill Watt, AMD, Si2 Low Power Coalition



Panelists discuss "SystemVerilog Design with Verification: Oil and Water Can Mix"

Chairman, "Introduction to the Low Power Coalition;" Qi Wang, Cadence, "Overview of CPF;" Gary Delp, LSI Logic, "Comparison of Power-Aware Formats: A User Perspective;" Rob Aitken, ARM, Library Considerations for Low Power;" Herve Menager, NXP, "End-User Experiences;" and Tom Miller of Sequence, Devadas Varma of Calypto, Dave Allen of Atrenta, and Anand K. Iyer of ArchPro, who all addressed "EDA Tool Development for Low Power."

AWARDS

Cadence was one of the recipients of the "Best Paper" award for "Period Optimization for Hard Real-Time Distributed Automotive Systems." The authors were Claudio Pinello of Cadence; Abhijit Davare, Qi Zhu, and Alberto Sangiovanni-Vincentelli of UC Berkeley; and Marco Di Natale and Sri Kanajan of General Motors.


Jan Willis, Senior Vice President of Industry Alliances at Cadence, was this year's recipient of the Marie R. Pistilli "Women in Electronic Design Automation" Achievement Award. Willis was presented with the prestigious award at the 12th Annual Workshop for Women in Design Automation (WWINDA) on Monday, June 4.



Low-power panelists discuss "Productivity Improvement and Risk Reduction"



Jan Willis accepts the Marie R. Pistilli Award



For more information about
this and other products contact:

info@cadence.com

or log on to:

www.cadence.com



cadence™

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS

2655 Seely Avenue

San Jose, CA 95134

P: +1.800.746.6223 (*within US*)

+1.408.943.1234 (*outside US*)

F: +1.408.943.5001

www.cadence.com