Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence Technologies and reference courses available worldwide. For exact course names, descriptions, and schedules, please refer to each regional course catalog on Cadence.com.

Contents

- PCB and Package Design with Allegro Technology
- Custom Design with Virtuoso Technology
- Silicon Sign-off and Verification
- Digital IC Design
- Verification across Languages, Methodologies, and Technology
- Acceleration and Emulation
- Tensilica Design IP
# Learning Map for PCB and Package Design with Allegro® Technology

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| **Master** | | | | |
| Allegro FPG System Planner (2) | Allegro GRE Interconnect Flow Planning (2) | Allegro Sigrity System-Level Serial Link Analysis (1) | | Allegro PCB Editor SKILL Language (3) |

| **Experienced** | | | | |
| Allegro Design Reuse (1) | Allegro Design Workbench for Engineers and Designers (1) | Allegro Sigrity Power-Aware Parallel Bus Analysis (2) | | Allegro Design Workbench for Administrators (2) |
| Allegro System Architect (1) | Allegro Team Design Authoring (1) | Sigtry PowerDC and OptimizePI (1) | | |
| Allegro PCB Router Basics (2) | Allegro PCB Editor Miniaturization Option (1) | Allegro Sigrity Package Assessment and Model Extraction (1) | | |

| **Core** | | | | |
| Allegro Design Entry HDL Basics (1) | Allegro Design Entry Using Orcad Capture (2) | Allegro Sigrity PI (1) | | Allegro PCB Librarian (2) |
| Allegro Design Entry HDL Front-to-Back Flow (3) | Allegro Design Entry Using Orcad Capture (2) | Allegro Sigrity SI Foundations (2) | | |
| Orcad CIS (1) | Allegro PCB Editor Intermediate Techniques (2) | Understanding High Frequency PCB Design: High-Speed, RF, and EMI (5) | | Allegro Design Workbench for Librarians (2) |
| Allegro PCB Editor Basic Techniques (3) | Allegro PCB Editor Basic Techniques (3) | SiP Layout (5) | | |

*NEW* Denotes Advance with Engineer Explorer course. L, XL, GXL denotes tiers of Cadence products used in course (not applicable if no legend).

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Also available online. Online only. EE Denotes Advance with Engineer Explorer course.
Learning Map for Custom Design with Virtuoso® Technology

IC CAD
- Advanced SKILL Language Programming (3)
- SKILL Programming for IC Layout Design (2)
- SKILL Development of Parameterized Cells (1)
- SKILL Language Programming (5)
- SKILL Language Programming Introduction (2)
- Virtuoso Design Environment Setup (1)

Analog, Mixed-Signal and RF Design
- Real Modeling w/ System/Verilog (2)
- Real Modeling w/ Verilog-AMS (2)
- Behavioral Modeling with Verilog-AMS or VHDL-AMS (2)
- Mixed-Signal Simulations Using AMS Designer (3)
- Virtuoso Electrically-Aware Design with Layout Dependent Effects (1)
- Virtuoso Analog Simulation (0.5-1.0 day short courses)
- Sensitivity Analysis & Circuit Optimization using ADE GXL
- Monte Carlo Sim. using ADE XL
- Creating Sweeps / Running Corners
- Intro. to the Virtuoso ADE XL Env.
- Virtuoso Analog Design Env. (3)
- Virtuoso Schematic Editor (2)
- Virtuoso Analog Design (3)
- Virtuoso Spectre Circuit Simulator (2)
- Virtuoso Spectre Pro (0.5-1.0)
- Transient Noise
- Accurate Fourier Transform
- S3: AC, XF, STB, Noise Analyses
- DC Algorithm
- Spectre Simulations Using Virtuoso ADE (1)
- Virtuoso Spectre Circuit Simulator (3)
- RF Analysis with Virtuoso Spectre Circuit Sim (3)
- Virtuoso Spectre Pro (0.5-1.0)
- Transient Noise
- Accurate Fourier Transform
- S3: AC, XF, STB, Noise Analyses
- DC Algorithm
- Spectre Simulations Using Virtuoso ADE (1)

Physical Design
- Analog-on-Top (AoT) Mixed-Signal Implementation (2) - uses IC and EDI
- Virtuoso Space-Based Router (2)
- Virtuoso Floorplanner (1)
- Using Virtuo Constraints Effectively (2)
- Virtuoso Connectivity-Driven Layout (2)
- Virtuoso Layout Pro (0.5 day short courses)
- Module Generator and Floorplanner XL, GXL
- Constraint-Driven Flow & Power Routing XL, GXL
- Interactive Routing XL
- Advanced Commands XL
- Basic Commands XL
- Create and Edit Commands L
- Environment and Basic Commands L
- Virtuoso Connectivity-Driven Layout Transition (1)
- Virtuoso Constraints Effectively (2)
- Virtuoso Connectivity-Driven Layout (2)
- Virtuoso Layout Pro (0.5 day short courses)
- Module Generator and Floorplanner XL, GXL
- Constraint-Driven Flow & Power Routing XL, GXL
- Interactive Routing XL
- Advanced Commands XL
- Basic Commands XL
- Create and Edit Commands L
- Environment and Basic Commands L
- Virtuoso Connectivity-Driven Layout Transition (1)

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NEW

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Learning Map for Digital IC Design

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Learning Map for Verification Across Languages, Methodologies, and Technology

**HDL Design and Verification with Incisive**

- **Real Modeling with SystemVerilog (2)**
- **SystemVerilog Register Verification using UVM (2)**
- **SystemVerilog Advanced Verification using UVM (5)**
- **Metric Driven Verification using Incisive vManager (3)**
- **Incisive Safety Simulator (2)**

**SystemC**

- **Specman Advanced Verification (4)**

**Specman**

- **Specman Fundamentals for Block-Level Environment Developers (5)**

**Core**

- **Verilog for VHDL Users (2)**
- **VHDL for Verilog Users (3)**
- **Verilog Language and Application (4)**
- **VHDL Language and Application (5)**
- **Incisive SystemC, VHDL and Verilog Simulation (2)**
- **Incisive SystemC Fundamentals (3)**
- **C++ Fundamentals for Design and Verification (2)**

**Experienced**

- **Verification with PSL (2)**
- **SystemVerilog Assertions (2)**
- **SystemVerilog for Design and Verification (5)**
- **Incisive Comprehensive Coverage with IMC (2)**
- **Incisive Debug Analyzer**
- **SystemC Synthesis with Stratus HLS (3)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

**Master**

- **Real Modeling with Verilog-AMS (2)**
- **JasperGold® Formal Fundamentals (3)**
- **Incisive Comprehensive Coverage with IMC (2)**
- **Incisive Safety Simulator (2)**
- **Specman Fundamentals (3)**
- **SystemC Synthesis with Stratus HLS (3)**
- **SystemC Transaction Level Modelling (TLM2.0) (2)**

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Learning Map for Acceleration and Emulation

**Core**
- Acceleration with Palladium XP (4)

**Experienced**
- SystemVerilog Advanced Register Verification using UVM (2)
- SystemVerilog Advanced Verification using UVM (5)

**Emulation**
- Power Aware Emulation with DPA and CPF (2)
- In Circuit Emulation with Palladium XP (3)
- Protium Rapid Prototyping Platform (1.5)

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Learning Map for Tensilica Design IP

**Communication**
- Tensilica ConnX BBE16 Baseband Engine (2)
- Tensilica ConnX BBE32EP Baseband Engine (2)
- Tensilica ConnX BBE64EP Baseband Engine (2)
- Tensilica ConnX BSP3 Bit Stream Processor (1)
- Tensilica ConnX SSP16 Soft Stream Processor (1)

**IoT**
- Tensilica Fusion DSP (1)

**Audio**
- Tensilica HiFi 3 Audio Engine ISA (1)
- Tensilica HiFi 2/EP/Mini Audio Engine ISA (1)
- Tensilica Audio Codec API (1/2 day)

**Imaging/Video**
- Tensilica IVP-EP Imaging and Video Processing DSP Platform (1)

**Core**
- Tensilica Processor Fundamentals (2)

**Experienced**
- Introduction to System Modeling with Tensilica Processor Cores (1)
- Tensilica Instruction Extension (TIE) Language and Design (1)

**NEW**
- Tensilica Fusion DSP (1)
- Tensilica HiFi 3 Audio Engine ISA (1)
- Tensilica HiFi 2/EP/Mini Audio Engine ISA (1)
- Tensilica Audio Codec API (1/2 day)
- Tensilica IVP-EP Imaging and Video Processing DSP Platform (1)
- Tensilica Instruction Extension (TIE) Language and Design (1)
- Tensilica Xtensa Processor Interfaces (1)
- Tensilica Xtensa Hardware Verification and EDA (1)

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