

# CADENCE KOREA ES SCHEDULE - 1st half of 2012

As of 2012-01-20

Course Name	Instructor	Product #	Length	S_Date	E_Date	Location
<b>Custom IC Design</b>						
Virtuoso Schematic Editor vIC 6.1.5	SCLEE	ES_84443_IC 6.1.5	2	01-11-12	01-12-12	Cadence Korea
Virtuoso Analog Design Environment vIC 6.1.5 & Virtuoso Spectre Circuit Simulator vMMSIM 10.1	SCLEE	ES_82083_IC6.1.5 & ES_84004_MMSIM 10.1	5	02-20-12	02-24-12	Cadence Korea
Virtuoso Analog Simulation Techniques vIC 6.1.5 (ADE-XL/GXL)	SCLEE	ES_84459_IC 6.1.5	2	02-27-12	02-28-12	Cadence Korea
Virtuoso Spectre Circuit Simulator vMMSIM 10.1	SWSEO	ES_84004_MMSIM 10.1	2	03-13-12	03-14-12	IT SoC
Virtuoso Analog Design Environment vIC 6.1.5	SWSEO	ES_82083_IC6.1.5	2	03-15-12	03-16-12	IT SoC
Virtuoso AMS Designer vIC6.1	SCLEE	ES_84468_IC6.1	3	03-21-11	03-23-11	Cadence Korea
SKILL Development of Parameterized Cells vIC5.1.41 (Pcell)	SYLEE	ES_84422_IC5.1.41	2	04-16-12	04-17-12	Cadence Korea
SKILL Language Programming IC5141 (SKILL)	YSOH/SYLEE	ES_83018_IC5.1.41	4	05-08-12	05-11-12	Cadence Korea
Virtuoso Layout Design Basics vIC6.1.5 (VLE-L)	SECHOI	ES_84460_IC6.1.5	2	05-14-12	05-15-12	Cadence Korea
Virtuoso Connectivity-Driven Layout vIC 6.1.5 (VLE_XL/GXL)	SYLEE	ES_84462_IC 6.1.5	2	05-24-12	05-25-12	Cadence Korea
Virtuoso Layout Design Basics vIC6.1.5 (VLE-L)	SECHOI	ES_84460_IC6.1.5	2	06-13-12	06-14-12	IT SoC
<b>Digital IC Design</b>						
Encounter Conformal ECO v10.1	DRSUH	ES_82194_10.1	3	02-20-12	02-22-12	Cadence Korea
Floorplanning, Physical Synthesis, Place and Route (Flat) v10.1	JGCHOI	ES_82160_10.1	3	03-07-12	03-09-12	Cadence Korea
Encounter RTL Compiler v10.1	WCRYU	ES_84441_10.1	3	03-19-12	03-21-12	Cadence Korea
SoC Encounter	JJLEE	ES_82160_10.1	2	05-03-12	05-04-12	IT SoC
CPF / Low-Power Verification with Encounter Conformal v10.1	DRSUH	ES_82156_10.1	3	05-16-12	05-18-12	Cadence Korea
Advanced Logic Equivalence Checking with Encounter Conformal EC v9.1	WCRYU	ES_82122_9.1	2	06-11-12	06-12-12	Cadence Korea
<b>Functional Verification</b>						
Incise Comprehensive Coverage v9.2	IJKIM	ES_82136_9.2	1	01-13-12	01-13-12	Cadence Korea
SystemVerilog Advanced Verification using UVM v1.0	DHBAE/IJKIM	ES_84497_1.0	4	02-14-12	02-17-12	Cadence Korea
Specman Elite Basics for Verification Environment Users & Developers v10.2	IHJUNG/SIMUN	ES_82138_10.1 & ES_82139_10.2	5	03-12-12	03-16-12	Cadence Korea
Incise SystemC, VHDL, and Verilog Simulation v9.2	ICJANG	ES_82115_9.2	3	03-28-12	03-30-12	Cadence Korea
SystemVerilog Language and Application v9.2(Design&Verification)	SIMUN/IJKIM	ES_82143_9.2	4	04-17-12	04-20-12	Cadence Korea
SystemVerilog Language and Application v9.2(SVA)	SIMUN	ES_82143_9.2	2	04-26-12	04-27-12	Cadence Korea
SystemVerilog Language and Application v9.2(Design&Verification)	ICJANG/DHBAE	ES_82143_9.2	4	05-15-12	05-18-12	IT SoC
SystemVerilog Language and Application v9.2(SVA)	IHJUNG	ES_82143_9.2	2	05-24-12	05-25-12	IT SoC
Incise Comprehensive Coverage v9.2	IHJUNG	ES_82136_9.2	1	06-15-12	06-15-12	Cadence Korea
Incise SystemC, VHDL, and Verilog Simulation v9.2	ICJANG	ES_82115_9.2	3	06-20-12	06-22-12	Cadence Korea
SystemC verification & Implementation with CtoS	JHPARK	ES_84496_10.2	3	06-25-12	06-27-12	Cadence Korea
<b>Silicon-Package-Board Co-Design</b>						
Allegro PCB Librarian v16.5	JHLEE	ES_86022_16.5	1	01-16-12	01-16-12	Cadence Korea
Allegro Design Entry HDL Front-to-Back Flow v16.5	JHLEE	ES_86015_16.5	1	01-17-12	01-17-12	Cadence Korea
Allegro PCB Editor Basic Techniques v16.5	JHLEE	ES_86097_16.5	2	01-18-12	01-19-12	Cadence Korea
Allegro PCB SI Foundations v16.5	JHLEE	ES_86046_16.5	2	02-23-12	02-24-12	Cadence Korea
Allegro Package Designer v16.5	JHLEE	ES_85022_16.5	2	03-26-12	03-27-11	Cadence Korea
Allegro PCB Librarian v16.5	JHLEE	ES_86022_16.5	1	04-23-12	04-23-12	Cadence Korea
Allegro Design Entry HDL Front-to-Back Flow v16.5	JHLEE	ES_86015_16.5	1	04-24-12	04-24-12	Cadence Korea
Allegro PCB Editor Basic Techniques v16.5	JHLEE	ES_86097_16.5	2	04-25-12	04-26-12	Cadence Korea
Allegro PCB SI Foundations v16.5	JHLEE	ES_86046_16.5	2	05-22-12	05-23-12	Cadence Korea
Allegro Package Designer v16.5	JHLEE	ES_85022_16.5	2	06-28-12	06-29-12	Cadence Korea

\* 4월 교육일정은 내부사정으로 일부 변경 될 수도 있습니다.  
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**\* Notes**

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3. 교육신청 마감

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