CUSTOMER SUCCESSES

METHODOLOGY

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Dear readers,

CDNLive! India 2006 which took place on October 12 was a big success, and I thank all of you who made the time to attend. Details of the event are given in this issue.

In October, Cadence made an important announcement with its new Logic Design Team Solution, which allows concurrent RTL design, enabling schedule predictability. This unique solution equips logic design teams with the elements they need—from verification and power to test and physical—plus plan-to-closure management and logical signoff in an integrated and holistic approach. It represents another deliverable in Cadence’s overall segmentation strategy, offering tailored solutions for specific types of engineering teams.

Cadence Design Systems and Silicon Integration Initiative (Si2), a worldwide consortium of industry-leading companies in the semiconductor, electronic systems and EDA tool industries, announced that they have reached agreement for Si2 to facilitate standardization of the Common Power Format (CPF) through the IEEE.

Also in this issue is an article authored by Dale Meehl and Tom Jackson on “Utilizing Volume Diagnostics Data to Improve Yield” that talks about Cadence’s Encounter Test solution.

Watch this space for details of the second annual Cadence Design Contest that will be launched soon!

Warm Regards,
Rahul Arya

We at Cadence, attribute the success of ICON to the overwhelming support of readers like you. It’s our constant endeavor to improve ICON, and we eagerly look forward to your valuable suggestions for the same.

Please write to Madhavi Rao at rmadhavi@cadence.com or call on +91 80 4184 1111
CDNLive! INDIA 2006

CDNLive! India 2006 took place at the Taj Residency on October 12 and was a huge success!

The day started with the plenary session where the guest keynote, entitled “Our World is Flat, and Round”, was delivered by Dr. Madhusudan Atre, Vice President & Managing Director, Agere Systems India. The talk focused on the evolution of the semiconductor industry and its future direction.

Dr Atre’s keynote was followed by the Cadence keynote by Cadence President & CEO, Michael J Fister. In his keynote presentation, entitled “Accelerating Innovation in an Accelerated Marketplace”, Mr Fister spoke about the emergence of 3 key markets – consumer, communication and computing (the 3C’s) - and introduced Cadence’s new Virtuoso 6.1 custom IC design solution.

The plenary session concluded with the announcement of the winner of the Cadence Design Contest – Shri Sant Gajanan Maharaj College of Engineering, Shegaon, Maharashtra. Their project, “Design and Implementation of Low-Cost Power Optimised OTA Based FPAA in 0.35 um Mixed-Mode CMOS Process”, was selected after a rigorous selection process by an expert committee comprising both industry and Cadence professionals. Congratulations to the SSGMCE team for a job well done!

After the plenary session, the conference program started in earnest, breaking into 4 parallel tracks with over 25 sessions including product roadmap presentations, customer and Cadence papers and the winning Design Contest and runner-up papers.

At the end of the conference program, the Best Paper Awards were announced. The recipients were:

- **Verification Track** – “Coverage Metrics and Module Verification Closure Using Model Checking” by Praveen Tiwari, Texas Instruments
- **Digital IC Track** – “An Innovative Flow To Implement Large Scale Design Changes At The Final Stages Of Physical Implementation” by Manoj Dadhich and Amit Bandlish, Freescale Semiconductor

The conference program was followed by an exhilarating entertainment evening courtesy the popular band Infrared, who had the entire audience on their feet with an energetic performance of old and new Hindi and English hits.

All in all, the event was a tremendous success, and if you weren’t there this year, make sure not to miss CDNLive! India 2007!

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CADENCE DESIGN CONTEST

In December 2005, Cadence launched an annual design contest and challenged engineering students to submit Analog/Mixed Signal/Digital design projects. The aim of the contest is to foster the spirit of inventiveness and realization of ideas. Undergraduate and graduate students from institutions that use predominantly Cadence EDA technologies were invited to participate.

The contest had a thorough elimination process that consisted of three stages. In the first stage, the teams were required to submit project papers, after which the shortlisted entries were asked to submit papers in IEEE (The Institute of Electrical and Electronics Engineers, Inc.) format, the standard format for submission of technical papers, to help them get a flavor of ‘real-life’ projects. In the final stage, the top 10 finalists presented their projects in September 2006 to a panel of experts that included prominent names from the electronic design industry including: S N Padmanabhan, vice president, MindTree Consulting; Anand Bariya, managing director, Netlogic Semiconductor; Dr. V Kamakoti, professor, IIT Chennai; and an expert team from Cadence India.

The contest attracted an overwhelming response. The quality of submissions was excellent and the judges were challenged to come up with the final shortlist.

In the end, it was the team from SHRI SANT GAJANAN MAHARAJ COLLEGE OF ENGINEERING, Shegaon, Maharashtra, who won the coveted first prize. Their project was entitled “Design and Implementation of Low-Cost Power Optimised OTA Based FPAA in 0.35 um Mixed-Mode CMOS Process.”

S N Padmanabhan from MindTree said, “The project was innovative and of a different nature compared to the rest of the entries. The dedication and enthusiasm of the students were great. They had surveyed similar products that are commercially available but took a different approach. The interest that their guide took in this project requires a special mention...the work is commendable”.

Congratulations to the SSGMCE team! Watch this space for the launch of the second design contest.

Mike Fister congratulates students from winning SSGMCE team
CADENCE ANNOUNCES WINNER OF ITS FIRST-EVER DESIGN CONTEST

Winner to present their project at CDNLive! India 2006

BANGALORE, India, October 11, 2006 — Cadence Design Systems (India) Pvt Ltd., the Indian subsidiary of Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced Shri Sant Gajanan Maharaj College of Engineering as the winner of the first-ever Cadence India Design Contest. Aimed at fostering the spirit of inventiveness and realization of ideas among the engineering student community in India, Cadence is the first company to organize a design contest of this nature in the region.

"The contest, an extension of the numerous initiatives by Cadence that nurture technical talent in electronic design in India, aims to challenge the student community and foster product innovation," said Jaswinder Ahuja, corporate vice president and managing director, Cadence Design Systems (India) Pvt Ltd. "We were pleasantly surprised by the overwhelming response received from engineering institutions, across India. This contest recognizes outstanding design achievements and encourages competitiveness among students and we hope to sustain the momentum in the future."

"We applaud Cadence for conceptualizing and launching such a contest. The judging process was rigorous and it forced our students to make sure their project was industry-standard. It was a great experience for the students to have such industry exposure and helps them to prepare for their future careers," said Shrikant Patil, Director, Shri Sant Gajanan Maharaj College of Engineering, Shegaon, Maharashtra.

The winning team will present their design to some of the brightest minds in the Indian electronics industry at CDNLive! India 2006, part of the Cadence global series of technical conferences, being held on October 12, 2006 in Bangalore.

The design contest invited participation from undergraduate and graduate students (B. Tech and M. Tech) from over 100 institutions that use Cadence technologies, as an extension of the company's University Relations program in India. Each project team comprised 2-5 students and a faculty member to guide them. Institutions that made it to the Top 10 include IIT Chennai, IIT Delhi, NIT Warangal, IISc and Jadavpur University.

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The shortage of design-aware manpower is a challenge that the semiconductor industry faces today. Cadence India focuses on a wide range of manpower-development initiatives including the Government of India’s Special Manpower Development Project, Cadence University Relations program, and the Finishing School Program, a certified advanced VLSI learning program for industry professionals.

CADENCE LOGIC DESIGN TEAM SOLUTION ADDRESSES FRONT-END DESIGN ‘PREDICTABILITY CRISIS’

Dramatically Simplifies Process of Managing and ‘Designing With’ Power, Verification, Test, and Physical Considerations; Reduces Project and Time-to-Market Risks

SAN JOSE, Calif., October 23, 2006

Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic-design innovation, today introduced the Cadence® Logic Design Team Solution, which allows concurrent RTL design, enabling schedule predictability. This unique solution equips logic design teams with the elements they need—from verification and power to test and physical—plus plan-to-closure management and logical signoff in an integrated and holistic approach. It represents another deliverable in Cadence’s overall segmentation strategy, offering tailored solutions for specific types of engineering teams.

Logic design teams are asked to create increasingly sophisticated products in shrinking geometries while meeting a growing range of design objectives, such as correct reusable functionality, power efficiency, functional quality, adequate testability, and physical feasibility among others. As design complexity has increased, the interdependency of these objectives has grown as well, limiting the scalability of today’s manual, sequential and highly iterative approaches. The result is a growing scheduling ‘predictability crisis’, in which changes made to improve one goal degrade the others, increasing project risks and schedule convergence challenges.

“Time-to-market pressure combined with growing design complexity offers up many challenges,” said Jerry Alston, senior vice president at QLogic Corporation.
“The combination of proven integrated front-end verification and implementation technologies for logic-design teams with a seamless linkage to system emulation enables us to stay ahead of the complexity curve. Our project teams clearly have an advantage taking this combination of front-end and systems approach, reduced overall product risk, and improved execution from architectural plan to logic design and verification to system-level closure.”

The Cadence Logic Design Team Solution integrates technology from the Cadence Incisive® functional verification and Encounter® digital IC design platforms. It integrates design, early verification and front-end implementation tasks into a set of objective-focused sub-flows, and automates the concurrent management of the design’s progress toward these objectives. The solution takes a concurrent ‘Design with’ approach—with early considerations for interdependencies and iterative flow aspects—as opposed to serial and highly iterative design. The architecture includes four major elements and an overall plan-to-closure management and logical sign-off solution, while leveraging industry-standard formats such as SystemVerilog. The Logic Design Team Solution includes:

**Design with Verification** – early design verification including assertion-based formal analysis, simulation and acceleration, and verification management

**Design with Power** – integrated low-power design and verification management across the front-end flow

**Design with Physical** – reduces logic-physical iterations by providing accurate estimates of timing using physical engines from implementation within the logic-design environment

**Design with Test** – integrates test with the logic-design environment to develop and debug high-quality test infrastructure with minimal iterations

**Design Logical Signoff** – comprehensive implementation handoff checks and analysis to verify front-end closure with predictability and confidence

**Design Management** – brings unparalleled predictability from plan to closure through an automated plan and metrics-driven management solution which tracks progress of the evolving design against all its functional, performance, and schedule objectives

“At Kawasaki Microelectronics, we rely on Encounter Test technology for the creation and production of deep submicron devices indispensable for the low-power consumer and high-performance information technology markets we serve,” said Yoshito Muraishi, director of CAD development at Kawasaki Microelectronics, Inc. “We are very pleased with the results of the Cadence Logic Design Team Solution, and with its Design with Test aspects. The deep level of integration and synergies between testability and synthesis, verification, timing analysis will further accelerate our time-to-market, reduce design iterations, improve shipped product quality and accelerate yield ramp.”

“The schedule predictability crisis is real,” said Ted Vucurevich, senior vice president and chief technology officer at Cadence. “We have been aggressively extending front-end technology and methodology innovation, building user-centric integrated flows and solutions across design and verification. The Cadence Logic Design Team Solution brings a practical and holistic approach to achieving predictability with an automated concurrent design process, replacing the ad-hoc serial, fragmented and manual approaches of the past.”

The Design-for-Test element will be featured at the International Test Conference in San Jose on October 24, 2006. Elements of the Cadence Logic Design Team Solution are described in more detail in the front-end design white paper at [www.cadence.com/whitepapers/frontend_logic_design.pdf](http://www.cadence.com/whitepapers/frontend_logic_design.pdf).

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**UTILIZING VOLUME DIAGNOSTICS DATA TO IMPROVE YIELD**

Dale Meehl and Tom Jackson, Cadence Design Systems

**Volume diagnostics**

Volume diagnostics analyzes results from wafer sort or final test utilizing failsets from automatic test equipment (ATE). These failsets include both input test patterns and measured miscompares on both scan and output pins. Typically, a batch diagnostics engine runs on parallel compute resources and will analyze hundreds, if not thousands, of failsets for a single device type. The diagnostics engines run fast and will accurately rate a set of faults for their correlation to each failset. In most cases, if the sample of failsets from a wafer lot is large enough, and if the failures are due to systemic issues, then the results would be accurate and show a high degree of commonality among failures.

Potential design and/or process fixes would then have a very high probability of being successful.

In the example described in this article, a semiconductor company utilized Cadence Encounter Diagnostics software to analyze results from their wafer electrical test (WET) process for a large nanometer device and found several common circuit elements involved in a substantial number of failing devices. This information was extremely helpful in their yield enhancement efforts. The failure sample size was hand picked after some basic human analysis and consisted of more than 400 failsets. After Encounter Diagnostics generated all callout data, several types of analysis were run against the data to find commonality among device failures.
Cell summary report

This report shows yield loss attributed to a specific cell type. There are several methods to normalize cell data including by die area, transistor count, and so on. In the specific case shown, normalization is by die area in cm² and instance count. The chart displays the most common failing cells within the wafer lots analyzed by Encounter Diagnostics.

Data from cell summary reports could direct design engineers to examine layout and placement locations of adjacent cells for the top failing cell types to ascertain if modifications should be made to either cell placement or inter-cell routing. Yield and process engineers may use this information to adjust recipes to tweak critical dimensions (CD) or implementation times on the highest failing cells to improve overall design yield.

Hierarchical summary report

This report shows the top macro failures within an IP block. As with the cell summary report, there are several methods to normalize this type of data. In this specific case, normalization of the data utilizes instance count.

Data from hierarchical summary reports could direct design engineers to examine layout and placement and to locate adjacent cells for the top failing IP blocks or the hierarchical level to ascertain if modifications should be made to either its placement or inter-cell routing. In the event of third-party IP usage, the report would be valuable when considering if the specific hard IP should be modified or even removed in the next iteration of the device.

Callout pin and net summary report

This report shows failures attributed to specific nets. As with the other summary reports, there are several methods to normalize this type of data including net wire length.

This report could guide layout engineers to examine the routing of those nets with a high failure rate. In addition, fab engineers could examine the metal layer where predominate failures occur to make metrology adjustments. This would also be valuable in prioritizing optical inspection for particular metal layers.

Failing test sequence report

This report highlights the failing test sequence that occurs most often.

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Failing test sequence report

This report highlights the failing test sequence that occurs most often.

This information, used in conjunction with other data and reports, would help guide yield enhancement efforts; engineers could sequence this test to the front of the test suite to optimize testing efforts.

Precision yield diagnostics

Volume diagnostics provides highly accurate samples of defect categories from its reports, which can pass directly to precision yield diagnostics (PYD). PYD is a methodology that provides more advanced analysis to determine the specific root cause of the most subtle nanometer design process interaction defects. PYD normally deploys to precisely locate the root cause defects in a given silicon die. In most cases, PYD can trace failures down to a particular interconnect wire. This information, in turn, drives various failure analysis (FA) processes to aid in both nondestructive and destructive exploration to point to the exact failure site/structure on a single die.

Conclusions

Ramping yield in a nanometer fab is essential, and today’s semiconductor companies are actively employing new techniques such as volume diagnostics in an attempt to locate and take action on faults caused by systemic design-process interactions. This paper shows a real-world example of this process and how design and fab personnel can use the information provided by volume diagnostics to improve yield.

Authors

Dale Meehl is a senior member of the consulting staff in the Cadence Encounter Test group. Prior to Cadence, Dale worked in EDA solutions for IBM Microelectronics. Dale has a B.S. in Electrical Engineering from Clarkson University.

Tom Jackson is currently a marketing director for the Cadence Encounter Test group and is responsible for diagnostics products. Tom has almost 20 years of EDA experience and began his career as a test engineer working on hardware accelerators. Tom has also held various positions in field applications and product marketing in the areas of design for test, formal verification, and yield management.
Design Platforms Address Power Optimization, Design for Manufacturing (DFM), Chip-Package Integration, and Design for Test (DFT) Challenges

SAN JOSE, Calif. and HSINCHU, TAIWAN , July 17, 2006

Cadence Design Systems, Inc. (NASDAQ: CDNS) and Taiwan Semiconductor Manufacturing Company (NYSE: TSM) today announced the integration of the Cadence® Encounter® digital IC design platform and Cadence Allegro® system interconnect platform into TSMC’s Reference Flow 7.0. With this reference flow, which supports designs targeting TSMC’s Nexsys™ 65-nanometer, process technologies, Cadence continues an established track record of innovation by improving its software for power optimization and analysis, design for manufacturing (DFM), chip-package integration, and design for test (DFT).

This latest milestone in the ongoing collaboration between the two companies delivers an RTL-to-package reference flow to accelerate time to volume for high-performance designs and low-power designs. The flow delivers a comprehensive methodology to address complex design issues at 65 nanometers, such as tight manufacturing parameters, an exponential increase in leakage power, and new extraction requirements. Within Reference Flow 7.0, Cadence technologies address these key issues by improving concurrent routing and dual-via insertion, adding new leakage power reduction strategies, addressing process-variation extraction issues, and continuing to optimize package performance and cost. Also within Reference Flow 7.0, Cadence is for the first time providing a complete RTL-to-GDSII and package flow, including all past and present TSMC Reference Flow capabilities for optimal customer referenceability.

“We worked closely with Cadence to meet the complex requirements that designers are facing at 65 nanometers, challenges such as power management, chip and package co-design, and manufacturing,” said Ed Wan, senior director of design service marketing at TSMC. “The Cadence track within TSMC’s Reference Flow 7.0 incorporates their technologies to lower the entry barrier for designers targeting TSMC’s advanced processes.”

“Reference Flow 7.0 offers comprehensive solutions to a complex 65-nanometer design. Manufacturing variance and accurate modeling are crucial for silicon design success at that node. Cadence provides a complete and integrated solution in TSMC Reference Flow 7.0 from low-power implementation, timing analysis to DFM and SSTA,” said Wei-Jin Dai, corporate vice president of Research and Development at Cadence. “The breadth of offerings and the capability to integrate into an easy-to-use flow is the key value that Cadence delivers to customers. Cadence also provides a 65LP tutorial and test case in the TSMC Reference Flow. Customers can download and walk through the complete flow with a real design.”

Power Optimization and Analysis

TSMC Reference Flow 7.0 continues to leverage key elements of the Cadence Encounter platform from Reference Flow 6.0, including voltage domain-aware technologies used to create power-gated paths and dynamic-voltage scaling, as well as path-specific power optimization using fine grain multi-threshold transistors (MTCMOS). Reference Flow 7.0 expands the range of power optimization options to include both coarse grain MTCMOS power gating and dynamic-voltage and frequency scaling. Designers can use these technologies not only to design with multiple supply voltages and power domains, leakage power and de-coupling capacitance optimization, automatic power-grid generation, and dynamic voltage (IR) drop analysis with actual IC package load models, but also to employ multiple modes of operation within a single block. The Encounter platform provides a scalable methodology to go from a non-power domain design to power-domain-based designs, as well as to choose between many options to maximize power optimization with acceptable area and/or performance.

Complementing this range of power optimization choices, the Encounter platform in Reference Flow 7.0 allows designers to perform multiple mode/multiple corner timing closure, automatic decoupling capacitor insertion, and dynamic IR analysis, taking into account all power optimization modes.

Elements of the Encounter platform within Reference Flow 7.0 include Encounter RTL Compiler global synthesis, Encounter Test, SoC Encounter system, Cadence QRC Extraction, VoltageStorm® Dynamic Gate power rail analysis, and CeltIC® Nanometer Delay Calculator (NDC), which work together to deliver high quality of silicon (QoS), improved timing closure, and reduced area.

DFM

Cadence SoC Encounter Global Physical Synthesis (GPS), which is included in Reference Flow 7.0, continues to provide solutions for critical manufacturing issues in the IC design process such as wire spreading, double-cut via optimization and metal fill. SoC Encounter GPS can automatically insert metal fill into a placed and routed design to achieve a metal density within the range recommended by TSMC design rules. It also enables automated wire-spreading and double-cut (dual) via insertion, which positively impact yield.
derive maximum theoretical yield. SoC Encounter DFY™ has been certified by TSMC as DFM compliant for CAA.

**Chip-Package Co-Design**
With Reference Flow 7.0, the Cadence Allegro platform continues the tradition of improving chip/package integration in TSMC Reference Flows such as the new capability of handling simultaneous switching outputs in timing and IR drop analysis. The flow also includes the capabilities to estimate the ratio of signal to power and ground bumps, estimate the number of vias needed on multiple planes in the package and estimate the number of decoupling capacitors needed in the package.

**DFT and True-Time Delay Test**
Encounter Test has been validated by TSMC in Reference Flow 7.0 to address at-speed and power-aware ATPG, at speed-and faster-than-at-speed test, and ATPG test compression. At 90 nanometers and below, test vectors themselves can cause dynamic IR drop issues during test - indistinguishable at first glance from a failed chip. Power-aware test allows an understanding of the magnitude and sources of power consumption via toggles in scan flos - thus permitting both re-architecture of test patterns to avoid problems and allowing scan-flop-specific optimization to reduce power impact. Faster-than-at-speed test allows testing of the design with a throughput higher than the tester clock rate, while ATPG test compression uses on-board logic to reduce the number of pins and test-applied vectors needed to achieve test coverage.

**Statistical Static Timing Analysis (SSTA)**
A new capability in Reference Flow 7.0 and the Encounter platform is statistical static timing analysis (SSTA) which uses a statistical distribution of cell timing/interconnect variance to determine the statistical distribution of timing of paths as would be expected in silicon. Cadence QRC Extraction is used to extract parameterized RC as a function of process variations, improving the performance and accuracy for SSTA. Using the advanced statistical modeling capability of Virtuoso® Spectre® Circuit Simulator, the process variation information provided by TSMC is accurately simulated and then converted into statistical cell timing models by SignalStorm-LC for statistical timing analysis.

**Availability**
TSMC Reference Flow 7.0 is available through the Company's customer web site, TSMC Online, or by contacting any TSMC account manager.

**About TSMC**
TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates two advanced 12-inch wafer fabs, five 8-inch fabs and one 6-inch wafer fab. TSMC also has substantial capacity commitments at its wholly owned subsidiaries, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. TSMC is the first foundry to provide 65-nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see [http://www.tsmc.com](http://www.tsmc.com).

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**ENCOUNTER RTL COMPILER CUSTOMER SUCCESSES**

Nethra Speeds Tapeout of Image Processor

Cadence and MIPS Technologies Deliver Encounter Reference Methodology for Industry’s Highest Performance 32-bit Core Family

Faraday Successfully Completes a Range of 130-nm Tapeouts with Cadence Encounter

Canon Adopts RTL Compiler For Faster Time to Better QoS and Requires ASIC Vendors to Support It