System / Verification: Formal Verification Track Abstracts

FOR201
Accelerating SoC Verification By Using Formal App’s in the DV Flow!!
Analog Devices

Siva Evani - Analog Devices
Ranga - Analog Devices

FOR202
Bugged by Register Verification? Let’s Get Formal
STMicroelectronics

Nitin Ahuja - STMicroelectronics
Pankaj Jain - ST Microelectronics
Vaibhav Mittal - Cadence Design Systems

In this paper we present the complexities associated with the verification of different types of registers used in the SOC and the limitation of simulation based verification to verify them. We present stimuli-less, quick, exhaustive and fully automated formal verification approach used for Register verification of ARM Cortex A53 based CPU Subsytem using JasperGold. Paper will enable the verification engineers to guarantee the complete functional verification coverage for registers while gaining on productivity as it presents a fully automated solution with minimal human intervention. Although the paper presents the methodology on ARM CPU based Subsytem, the methodology is very well scalable from IP level to complete SOC.”
FOR203
Formal VIPs for Effective Verification of Standard Design Components
Nvidia

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Siddartha Papineni - Nvidia
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While the complexity of design is increasing exponentially, multiple modules across chips continue to use certain basic building blocks like fifos, arbiters, along with standard interfaces like the credit/valid, axi, etc. Since each of these building blocks are part of various modules in chips, redundant work is being done to verify the same logic which may not be comprehensive / complete solution. It is important to have recipe in the form of a VIP suite to address verification of the standard building blocks and the glue logic surrounding it. In this session we will discuss a library of such VIP checks that can be cleanly instantiated in the RTL as well as in the verification test-benches. These checkers can be used for verification either through simulation/formal verification.

FOR204
Bug-Hunting in a Processor Design by Formal Verification Techniques
Analog Devices

Mohammadi Bharmal - Analog Devices
Sri Ranganayakulu - Analog Devices
Saurbh S - Analog Devices

The biggest challenge in functional DV of a complex digital system is to ensure 100% functional coverage by generating all the legal vectors and ensuring that the system behaves as specified for all these vectors. However, if the behavior of the system is well defined for all the vectors, formal verification (FV) techniques can help in proving that the desired behavior will always be observed, for all the legal vectors. This paper highlights how FV can be used in verification of a complex processor core; and also the strategy, experiments and results of a project, using Cadence IEV and Cadence AXI ABVIPs and in-house assertions for FV of a complex processor. The techniques presented in this paper could be deployed by designers to propel the verification or by verification engineers to sign-off the verification, for any complex digital system.
FOR205

CSR Formal Validation: A Step Close To Closure and Higher Confidence

Qualcomm

Mohammad Tauqueer Alam - Qualcomm
Maruthi Srinivas - Qualcomm
Suresh Babu Juluri - Qualcomm
Ravi Marate - Cadence Design Systems

Complex core top CSR (TCSR) provides control register for all power collapsible subsystems, special registers for software to pass control among different CPUs, central interrupt, status registers for all security related violations. It also has a collection of miscellaneous registers for top level control. Access control to all TCSR is protected by two security module configured. In this session, we will share both our experiences in utilizing fully automated CSR flow from Jasper for production design usage and also a new capability in jasper in validating special register. We will discuss the pros and cons of each and share our practical recommendations for production usage.

FOR206

Solve the Mainstream Functional Verification Challenges Using Smart Formal Verification Approaches

Texas Instruments

Harish M - Texas Instruments
Ashwini Padoor - Texas Instruments

Increasing size of design and reducing time to market for SOCs, puts pressure on verification. This requires us to use differentiating techniques for shortening verification cycle and improving quality of designs. This session describes on the usage of formal verification to quicken the verification cycle. The formal verification apps and user defined assertion has been deployed successfully to improve the verification quality as well as to obtain the verification metrics in an efficient automated way. The paper provides complete outline about the various techniques which we have integrated in our verification process. The same approach has been extended to IP verification as well into SOC verification flows.
FOR207
Slice System – SoC Level Inter Connection Extractor
Qualcomm

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Maruthi Srinivas - Qualcomm
Ambudhar Tripathi - Qualcomm
Thomas, Vineeth - Qualcomm

If you have worked on SoC integration, you need to know the latest methods used for effective connectivity reviews. If you work on an IP team, you will learn how to remove unnecessary loopbacks and save on the number of wires in physical design. You will also learn to compare connectivity across chips on a SoC platform. You can bid adieu to late functional ECOs arising from incorrect connectivity. As a SOC process, you have to do the connection review with IP teams. The conventional way of doing this is quite clumsy and there is a good chance that connectivity issues be missed. This is because conventional files used for reviews are not informative and comprehensive enough for IP designer to identify issues. In this session, you will learn how to generate connectivity statistics; categorize, review and compare connectivity changes faster – as well as document changes for future use, through a formal approach.

FOR208
Sequential Equivalence Check for Context Switching Verification With JG SEC App
Nvidia

Tushar Kanti Biswas - Nvidia
Dheeraj Ameta - Nvidia
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Prosenjit Chatterjee - Nvidia

With evolution of computing technology, there is an ever increasing demand for support of highest degree of multitasking. A context switch is the process of saving and restoring the state (context) of a process, so that execution can be resumed from the same point at a later time. Every time a context switching occurs, context information of running process is saved into a memory and context information of next process is retrieved from the memory. While saving the context information, it is always a concern whether we have saved enough information, so that upon retrieving them we can resume a process from the point where we had left it earlier. In the session we will discuss about a method through which we can verify this formally, with help of JG SEC App.
FOR209
NOC Functional and Deadlock Verification Using Formal
Qualcomm

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Nirmal Arumugam - Qualcomm
Maruthi Srinivas Narasimhan - Qualcomm
Supriya Bhattacharjee - Qualcomm

The increase in SOC connectivity between various blocks and addition of new blocks on
the Network is continuously making the task of exhaustively verifying the Network On
Chip (NOC) very difficult and time consuming. The increase in complexity and reduction
in time-to-market calls for a migration from traditional simulation technique of
verification to formal verification for an effectively trustworthy verification result. The
presentation will be focusing on the details about the issues faced while using simulation
techniques for NOC verification which will eventually be leading to the advantages of
using formal verification techniques for the same. Also, it will touch up on the topics of
the essential points required to bring up the setup to start with the verification along
with some enhancements (still under discussion) for a comprehensive testing to
eliminate any chances of bug being left in the silicon.