Processor Optimization with ARM POP and Cadence Flow

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### ARM’s POP Unique Position

- **Co-development by Processor and Physical IP Division**
  - Intimate R&D efforts by internal teams, unmatched any other provider
  - First with new cores and new process geometries

- **Best CPU configuration**
  - Based on thorough benchmarks
  - Recommended configuration bring 80% more efficiency
Strong Partner Adoption of POPs

“Panasonic licensed the ARM Processor Optimization Pack (POP) to achieve up to 1.4GHz performance for our ARM Cortex-A9 based SoC,” said Masaitsu Nakajima, General Manager of Processor Core Technology at Panasonic. “ARM EDA tool support and production-ready physical IP helped accelerate our time-to-market.”

- 28 POP licenses to date
- Repeat customers already achieved
Processor Optimization Pack “POP”

Optimize for Performance on Power
Comprehensive Implementation Solution
Silicon Proven Results
Fast Time to Market

Achieve up to 25% increase in performance or more than 80% reduction in leakage power
<table>
<thead>
<tr>
<th>What’s in PoP: Physical IP for Specific Node</th>
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<tbody>
<tr>
<td><strong>SC12MC High Performance Multi-Channel Library</strong></td>
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<tr>
<td>➔ Architected to provide leakage recovery</td>
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<tr>
<td><strong>SC12MC High Performance Kit – HPK</strong></td>
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<tr>
<td>➔ Built specifically for Cortex-A9 / A5 enabling high performance, and lower power</td>
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<tr>
<td><strong>SC12MC Power Management Kit – PMK</strong></td>
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<tr>
<td>➔ Aligned with ARM CPU power management schemes</td>
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<td>➔ Interoperable with leading EDA tools</td>
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<tr>
<td><strong>Fast Cache Instance – FCI (including overdrive support)</strong></td>
</tr>
<tr>
<td>➔ Built specifically for Cortex-A5 &amp; A9 enabling high performance, low leakage power, and enhanced DFT</td>
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</tbody>
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Physical IP platform on TSMC 40LP
No hidden agenda

- Datasheet provides (example shown across)
  - CPU Core configuration
  - Performance
    - unmargin
    - with % OCV
  - Leakage
  - Dynamic Power using Dhrystone vectors
  - Margins
    - OCV
    - Clock uncertainty
    - PLL Jitter, duty cycle variation
  - Physical details
    - Floorplan size
    - RAM size
    - Utilisation
    - Power grid & IR Drop
- Main objectives
  - Consistency and technical creditability
  - PPA numbers that are manufacturable
  - ARM keeps the database at hand to allow further support / questions on trial implementation

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![Cortex-A9 GHz Results in Production](chart.png)

Typical silicon results


POP User Guide

- ARM publish a user guide for each POP
  - Architectural details specific to Cortex-A9 implementation.
    - References to flow, RAM timing
  - Physical Optimisation
    - Floor planning, bounds, how to get predictable placement results
  - Flow approaches and methodology
    - Don’t use lists, Library use strategy, Sprinkle-(G) / Backfill(LP)
  - Timing Optimisation & Sign off criteria
    - Sign-off, Path Groups and ECO flows
- User guide connects the reference flow with the process specific techniques and results achieved in ARM’s benchmarking activity
ARM PoP Benefits

**GHz + Guarantee with Low Power**
- Path to predictable PPA
- Silicon Proven Results
- Industry Lowest Power implementation!

**Best efficient system configuration**
- 80% more efficient on L2 access

**Rapid time to reproduce**
- Easy reproduction within two to four weeks
- Reduce $$ spent on service providers and EDA tools

**Opportunity to differentiate**
- Knowledge transfer
- Methodology expandable to different configuration
Challenge:

Implement an ARM® Cortex™-A9 on TSMC 40LP process

_in 12 Weeks!

Mission
Impossible?
With Design Complexity Increasing:
How do you predict the target?

Engineering Challenges

• Architectural planning
• Floorplan analysis
• EDA tools and flow
• Physical IP

Engineering Performance and Power Target

• Active performance Dhrystone
• Power mW per MHz
• Standby power
Cadence is Working With ARM to Help You Overcome This Challenge
ARM’s Processor Optimization Pack
Using the Latest Cadence Encounter Tools

“Outsource” engineering and design risk

- High performance
  - ARM Cortex-A9 POP using latest Cadence Encounter® Digital Implementation EDI (System) tools delivers market-leading performance

- Rapid time to market
  - ARM’s detailed implementation guide provides knowledge transfer supported by Cadence experts

- Certified benchmarked data
  - Detailed power, performance, and area (PPA) target to help set design goals

- ARM’s core-optimized Physical IP
- Proven with a Cadence flow
Cortex-A9 Performance Trend

- Cadence PPA Team
- Target

<table>
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<tr>
<th>Week 1</th>
<th>Week 2</th>
<th>Week 3</th>
<th>Week 4</th>
<th>Week 5</th>
<th>Week 6</th>
<th>Week 7</th>
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CCOpt-Enabled
ARM Implementation Guide
Cadence Hand-Tuning
CCOpt Advantage
Analysis based on postRoute DB

Performance improved 17.45%
745MHz → 875MHz

Slack

Power

Traditional CTS
CCOPT

-0.4
-0.3
-0.2
-0.1

520mA
540mA
560mA
580mA

520.20
567.90

Dynamic: 8%
ARM and Cadence have a long-standing collaboration to integrate high-performance ARM processors into advanced node designs

- The aim of the collaboration is to accelerate the design process to help our customers achieve their PPA goals while meeting design schedules

- We’ve recently added a focus on integration of ARM Cortex-M processors into embedded mixed-signal applications using Cadence Virtuoso® mixed-signal design solutions

- Internally, ARM uses Cadence tools and flows for development of high-performance processors, GPUs, and mixed-signal IP blocks
For Further Information

• Come and see ARM present detailed information on its POP products and roadmaps at the Cadence EDA360 Theaten

• For more technical information and details of ARM Processor Optimization Packs from ARM and Cadence, please contact James Davey – Jdavey@Cadence.com or Ron Moore – Ron.Moore@ARM.com