

R&D in SH

1. Senior Software Engineer for Physical Design Rule

Job Description

- Responsible for developing and maintaining physical verification engine in EDI systems.
- Responsible for implementation for physical design rule check of advanced node process.
- Responsible for performance improvement in current physical verification engine.

Job Requirements:

- The candidate should be very strong at complex software development with C or C++ on UNIX platform, domain knowledge at Physical Design Rule Checking is preferred.
- The candidate will be responsible for development of complicated algorithms to check design rule violation among huge geometries, the experience to handle large data manipulation is preferred.
- Experienced in software development with MS or PHD degree of CS/EE/Math or others related.
- Good team player with strong written and verbal communication skills
- Familiar with LEF/DEF is preferred, and the ability to geometrical operation is definitely a plus.

2. Senior Engineer for Power Route

Job Description:

- This position is for a R&D engineer to assist in development of special routing (power planning / power routing ...) solution of digital IC design in Encounter.
- The candidate will be responsible for designing, developing, troubleshooting and debugging software programs of routing flow and related algorithms.

Position Requirements

- Have strong software programming skill with C/C++ on Linux/Unix platform.
- Require candidate have strong desires to learn and to explore new technologies
- able to demonstrate good analysis and problem solving skills
- EDA software development experience or IC design knowledge, especially in backend
- Know basic routing algorithms.
- Good English communication skill, both oral and written.

3. Senior Software Engineer for GUI

Position Description:

- The candidate will be responsible for the development and maintenance of GUI and system infrastructure of Encounter platform in Cadence.

Position Requirements:

- MS or above in CS/EE or similar fields with 3+ years of working experience or BS with 5+ years of working experience for Sr. Member of Technical Staff;
- Programming skill on Linux/Unix platform is must.
- Strong C/C++ language coding skill.
- Being Familiar with GUI application development, such as Open GL, Qt, tcl/tk, X
- Good understanding on algorithm.

- EDA software development experience is a plus.
- Good English communication skill, both oral and written.

4. Senior Software Engineer (Database development for Encounter platform)

Position Description:

- The candidate will be responsible for the development and maintenance of Database of Encounter platform in Cadence. The engineer works with engineers in Shanghai and US.

NOTE: The database is a specific designed one for back-end EDA tools, NOT a general relational database with SQL.

Position Requirements:

- MS or above in CS.
- Programming skill on Linux/Unix platform is must.
- Deep understanding on Linux OS
- Strong C/C++ language coding skill.
- Having Sound experience in software development projects and a strong background in data structures, algorithms and program design.
- Tcl programming skill is a plus.
- Multiple thread programming experience is a plus.
- EDA software development experience or IC design knowledge is a plus.
- Strong desires to learn and explore new technologies and is able to demonstrate good analysis and problem solving skills
- Good English communication skill, both oral and written.

5. Senior Software Engineer for Floor plan

Position Description:

- The candidate will be a member of the Encounter floorplan team in Shanghai, to work on the development and maintenance of manual Floorplan project.
- The responsibilities include the development of new features and products, and support other teams in Encounter product lines.
- The candidate must be comfortable working with existing code as well as developing new functionality to address new requirements, and be working closely with local/remote team members, and be also strong technical support to team.

Position Requirements:

- Candidate must be an expert in software engineering methods and committed to high quality of development work.
- The individual must be team-oriented, possess good communication skills, self-motivated, able to work independently and working with a team from multiple remote sites.
- Candidate must be able to develop detailed technical specification as well as the ability to scope efforts required.
- The candidate must be also smart to capture new EDA technologies, and switch among different areas successfully.
- Advanced developing and debugging software in UNIX & LINUX environments, familiar with gnu c/c++, gdb etc..
- Strong problem-solving, architecture, algorithmic.
- Familiar with interpreted language such as TCL is a plus.

- Knowledge of Digital Physical Design flow such as Floorplan/Placement/Routing/CTS is a plus.

6. Senior Software Engineer for Encounter Hier Solution Team

Position Description:

- The candidate will be a member of the Encounter Hier Solution team in Shanghai, to work on the development and maintenance of Hier Solution project.
- The responsibilities include development of new features and products, and support other teams in Encounter product lines.
- The candidate must be comfortable working with existing code as well as developing new functionality to address new requirements, and be working closely with local/remote team members, and be also strong technical support to team.

Position Requirements:

- Candidate must be an expert in software engineering methods and committed to high quality of development work.
- The individual must be team-oriented, possess good communication skills, self-motivated, able to work independently and working with a team from multiple remote sites.
- Candidate must be able to develop detailed technical specification as well as the ability to scope efforts required.
- The candidate must be also smart to capture new EDA technologies, and switch among different areas successfully.
- Advanced developing and debugging software in UNIX & LINUX environments, familiar with gnu c/c++, gdb etc..
- Strong problem-solving, architecture, algorithmic.
- Familiar with interpreted language such as TCL is a plus.
- Knowledge of Timing analysis is a plus.

7. Senior Software Engineer for

Position Description:

- R&D engineer to do the clock tree synthesis related works (product maintain, software development, design flow improvement etc.)

Position Requirements:

- MS or PhD in EE/CS etc.
- Excellent programming skills (C/C++, script)
- The following background is preferred: EDA, IC physical design, CTS, Timing analysis, Optimization.
- Good written and spoken English
- Good communication skills and be able to work within a team.

8. Sr. Member of Technical Staff for

Position Description

- Seeking software engineer to develop and debug software addressing Design for Manufacturability (e.g., lithography, CMP)

Position Requirements

- Candidate must be familiar with software engineering methods and committed to high quality of development work. The individual must be team-oriented, possess good communication skills, self-motivated, able to work independently and working with a team from multiple remote sites. Candidate must be able to develop detailed technical specification as well as the ability to scope efforts required.
- B.S. In CS, EE, or equivalent fields with competency in object-oriented language programming
- Strong analytical skills, systematic thinking, and problem-solving minded; can work creatively and independently on a larger scale problem set
- Industry experience in programming or PE (scripting) work related to geometry-based signoff tools such as DRC and RCE
- Exposure to lithography and/or CMP technology, lithography-related and/or CMP EDA tools is preferable

9. Lead PV Engineer

Position Description

- We are looking for an engineer/designer with the desire to perform product validation on our Signal Integrity products. You will be responsible for testing and overseeing the quality management of our family of software products that deal with high speed signal design.
- Duties include working within a multi-functional global project team, review and develop automated tests within the existing test environment, review project plans and functional specifications, develop test criteria and written test plans, manually exercise and test functionality of the Allegro SI product.

Position Requirements

- B.S. with 2+ years in related work experiences
- Knowledge in Signal Integrity analysis, such as Bus Analysis, SSN, Crosstalk and Power Analysis.
- English are mandatory as the candidate will be interacting with a global team.
- Excellent debugging skill
- Knowledge of Cadence Allegro platform is a plus
- Knowledge of other high speed tools is a plus
- Knowledge in Printed Circuit Board design is a plus
- Experience with Perl, Java or other programming languages is a plus
- Familiar with UNIX and Window systems

10. Senior Software Engineer for FPGA

Position Description

- Responsible for designing and developing sub-systems and modules or components of hardware based verification products. In addition modifying, updating and productizing existing hardware based verification products. Perform as individual contributor on FPGA based design projects involving board design, RTL design, verification, productizing and documentation. Work on diverse problems related to FPGA design, simulation or verification issues.

Position Requirements

- The position requires BS/EE, or equivalent, with a minimum of 4 yrs of industry experience in designing hardware systems.
- Must have excellent communication skills, both written and verbal.

- Technical expertise in FPGA design for either Altera or Xilinx products is required.
- Experience in FPGA design methodologies including high speed design, serial protocols and FPGA timing closure is desired.
- In addition RTL design knowledge using Verilog is required along with experience in using RTL verification tools and flows.
- Verification using Cadence simulation products is desired.
- Experience with scripting languages like Perl, TCL C-shell is strongly recommended.
- Experience with PCB tools is also desired. Experience with high speed memory interface design is also desired.

Product Engineer in SH

1. Senior Product Engineer for CTS

Position Description

- Responsible for Encounter tools including CTS.
- Work with R&D closely, to analyze/build/debug design flow to help R&D to improve Encounter tools performance and QoR on complex digital implementation design flow.
- Plan and develop product spec for EDA tools to address future and immediate customer requirements.
- Interface with cross-function team to create technical solutions, involve in customer engagement.

Position Requirements

- CS/EE BS degree with 5+ years or MS degree with 3+ years of EDA or IC design related experience.
- Good experience with CTS, Place and Route design flow using EDA tools.
- Be familiar with IC back-end design flow, from netlist to gdsout.
- Strong analysis/debug capability for technical issues, be detailed oriented with a focus on quality.
- Good team player with strong written and verbal communication skills.
- Be able to work under pressure, be able to work on multiple projects at the same time.
- Good English read, write and communication Skill.

2. Product Engineer for Lib-QA

Position Description:

- Responsible for physical library qualification in Encounter products including Nanoroute.
- Work with R&D closely, to analyze/build/debug design flow to help R&D to improve Encounter tools performance and QoR on complex digital implementation design flow.
- Plan and develop product spec for EDA tools to address future and immediate customer requirements.
- Interface with cross-function team to create technical solutions, involve in customer engagement.

Position Requirements:

- CS/EE BS degree with 5+ years or MS degree with 3+ years of EDA or IC design related experience.
- Good experience with Place and Route design flow using EDA tools. Good knowledge of LEF/DEF.
- Be familiar with IC back-end design flow, from netlist to gdsout.

- Strong analysis/bedbug capability for technical issues, be detailed oriented with a focus on quality.
- Good team player with strong written and verbal communication skills.
- Be able to work under pressure, be able to work on multiple projects at the same time.
- Good English read, write and communication Skill.

3. Senior Product Engineer for power planning and routing

Position Description:

- Power planning and routing are essential technologies for chip design. EDI has comprehensive power planning and routing capabilities for power ring, stripes and mesh generation and optimization. The tools and features are widely use by worldwide customer for cutting edge technologies and designs. This position requies candidates to work on complicated power planning and routing technologies with customer and consolidate the requests into tool features to upgrade customer productivity.

Position Requirements:

- Master on EE/Microelectronics + 2-3 years of working experience
- Worked on IC back-end design
- With usage experience of Encounter/ICC for floorplan, power planning, power routing and low power design is highly appreciated
- Good communication skills to work with both customer and RD group
- Good capability to work out generic solution to cover requests from various customers
- Quicker learner for new technology and large amount of knowledge
- Good English for writing and presentation

4. Product Engineer of flipchip solution using Cadence IC design tools

Position Description:

- ICD provides a set of design tools for flipchip design including flipchip floorplan, flipchip routing, point to point router, wire editor and verification. With the increment of customer requests, a product engineer is needed to work on the tool development, function definition and verification, customer support and co-work with development team.

Position Requirements:

- CS/EE BS degree with Flipchip IC support related experience.
- Good experience with package design with EDA tools.
- Be familiar with IC back-end design flow, for floorplan, powerplan, special route, etc.
- Strong analysis/bedbug capability for technical issues, be detailed oriented with a focus on quality.
- Good team player with strong written and verbal communication skills
- Be able to work under pressure, be able to work on multiple projects at the same time.
- Good English read, write and communication Skill

5. Product Engineer for QoS

Position Description

- This job is an important addition to Encounter quality and performance
- Responsible for QOS analysis and debug for EDI whole backend flow, from floorplan to final SI timing closure
- Responsible for CPU and memory qualify maintain during regular review
- Continuously to add and tune large scale and advance node designs into QoS suite

- Working closely with other team members for technique communication and projects. Can take lead role in project plan and action.

Position Requirements

- MS with EE background, previous experience on EDA tools and frontend/backend design is a strong plus
- Excellent knowledge at backend flow in digital design, including placement, optimization, cts, route and SI, which is the most important for this job.
- Excellent knowledge at timing analysis, good at power analysis and low power.
- Be familiar with software development process, debugging tools, and configuration management concepts.
- Know well about verilog, simulation, dft, dfm.
- Excellent ability to learn, explore and strong ability in solving problems independently.
- Good team working attitude and innovating spirit.
- Good Chinese and English communication skills.

6. Senior Product Engineer for QoS

Position Description

- This job is an important addition to Encounter quality and performance
- Responsible for QOS analysis and debug for EDI whole backend flow, from floorplan to final SI timing closure
- Responsible for CPU and memory qualify maintain during regular review
- Continuously to add and tune large scale and advance node designs into QoS suite
- Working closely with other team members for technique communication and projects. Can take lead role in project plan and action.

Position Requirements

- BS with minimum 5 years and MS with 3 years working experiences. EE background, previous experience on EDA tools and frontend/backend design is a strong plusExcellent knowledge at backend flow in digital design, including placement, optimization, cts, route and SI, which is the most important for this job.
- Excellent knowledge at timing analysis, good at power analysis and low power.
- Be familiar with software development process, debugging tools, and configuration management concepts.
- Know well about verilog, simulation, dft, dfm.
- Excellent ability to learn, explore and strong ability in solving problems independently.
- Good team working attitude and innovating spirit.
- Good Chinese and English communication skills.

Product Validation in SH

1. Senior PV Engineer (Digital Backend) ×4 Vacancies

Position Description:

- This job is an important addition to our R&D team to develop Cadence Encounter Digital Implementation System (EDI)
- Responsible for developing, applying, and improving quality standard for Cadence EDI products
- Required to acquire expertise and ownership over existing product components as well as develop brand new product features.
- Help identifying new technology challenges in advanced process nodes and proactively provide the product improvement suggestion to R&D
- Build up EDI expertise and deliver support to field team and customers whenever needed

Position Requirements:

✓ **Experience:**

- BS with minimum 2.5 years or MS with 1 year work experiences
- EE/MicroEE/Physics background
- Previous working experience in Fab, EDA industry, or design house would be a strong plus
- Excellent new graduate with good academic background or industry internship experience can also be considered.

✓ **Knowledge:**

- Digital Backend Design knowledge are highly preferred
- Experience with Digital Backend EDA Tool (Encounter, ICC etc.) or STA tool (Encounter Timing System, PrimeTime) would be a strong plus
- Candidate must have excellent capability to learn, explore and solve problems, have team-cooperating and innovating spirit,
- Candidate must possess good Chinese and English communication skills;

2. Lead PV Engineer

Position Description:

- This job is an important addition to Encounter quality and performance
- Responsible for QOR analysis and debug for EDI whole backend flow(后端流程), from placement to final SI timing closure
- Responsible for CPU and memory qualify maintain during regular review
- Continuously to add and tune large scale and advance node designs into validation suite
- Working closely with other team members for technique communication and projects. Can take lead role in project plan and action.

Requirements:

- BS with minimum 6 years and MS with 5 years working experiences. EE background, from design house or EDA company is strong plus.
- Be familiar with software development process, debugging tools, and configuration management concepts.
- Excellent knowledge at backend flow in digital design, including placement, optimization, cts, route and SI, which is the most important for this job.
- Excellent knowledge at timing analysis, good at power analysis and low power.
- Know well about verilog, simulation, dft, dfm.
- Excellent ability to learn, explore and strong ability in solving problems independently.
- Good team working attitude and innovating spirit.
- Good Chinese and English communication skills.

3. Senior PV Engineer for PVS

Position Description

- This job is an important addition to our R&D team to develop PVS.
- Responsible for developing, applying, and maintaining quality standard for PVS related technology and products.
- Responsible for testing PVS in all kind of Virtuoso/Encounter/K2 design flow.
- Required to acquire expertise and ownership over existing product components as well as develop entirely new product features.
- Work with other engineers as a team and help to provide feedback when required.

Position Requirements

- BS with minimum 2.5 years or MS with 1 year work experiences. EE background, from design house or EDA Company or fab is strong plus. Excellent new graduate can also be considered.
- Prior experience in Physical verification is desired. Be good at usage of mainstream Cadence/Synopsys/Mentor Assura, Hercules, Calibre tools.
- Be familiar with software development process, debugging tools, and configuration management concepts is a plus.
- Candidate must have excellent ability to learn, explore and solve problems, have team-cooperating and innovating spirit,
- Candidate must possess good Chinese and English communication skills;

4. Lead PV Engineer for QOR

Position Description:

- Run QOR regression on multiple design suites daily and weekly to catch QOR/Performance issues in time, debug and file bugs to RD for QOR degradations.
- Take projects from RD or PE requests in validating code changes.
- Add and tune designs into current suite, including advance technology designs and larger designs.
- Develop system using scripts such as cshell, perl or tcl.

Position Requirements:

- BS with 4 years or MS 2years of EE background, from design house or EDA Company or fab is strong plus.
- Know good at APR flow, such as placement, route, cts, optimization, xtalk etc.
- Be familiar with software development process, debugging tools, and configuration management concepts.
- Candidate must have excellent ability to learn, explore and solve problems, have team-cooperating and innovating spirit,
- Candidate must possess good Chinese and English communication skills;