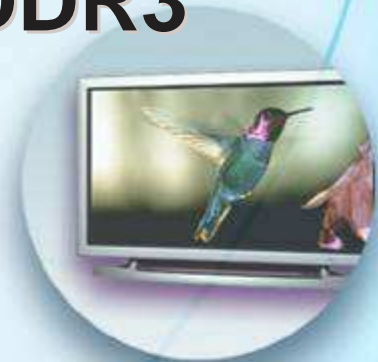




Challenges in Implementing DDR3 Memory Interface on PCB Systems - A Methodology for Interfacing DDR3 SDRAM DIMM to an FPGA



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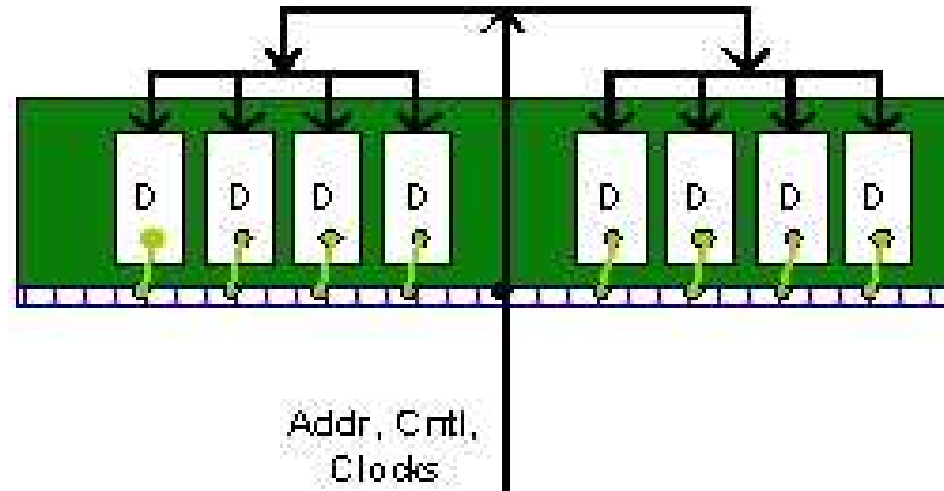
Roadmap

- Migration from DDR2 to DDR3
- DDR3 read/write leveling
- Methodology for setup and analysis of DDR3 interfaces

Migration to DDR3

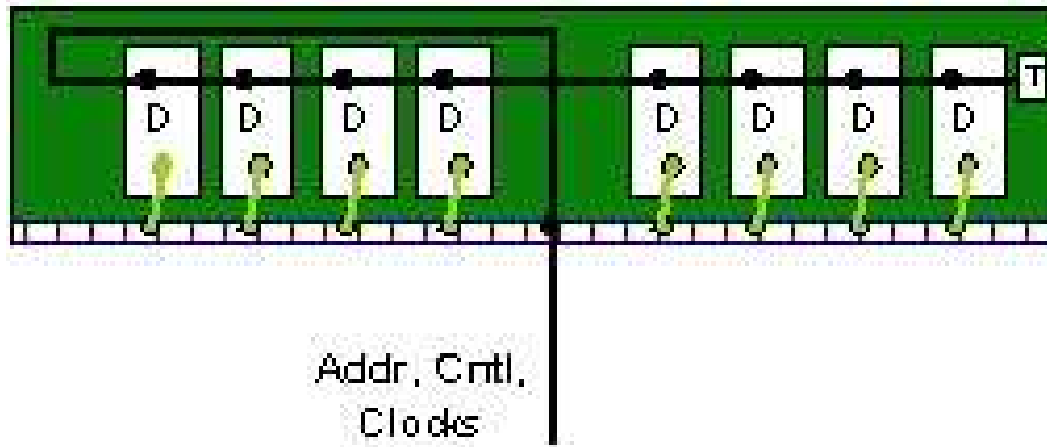
	DDR2 DIMM	DDR3 DIMM
Data Rate	400-800 Mbps	800-1600 Mbps
Voltage	1.8V SSTL	1.5V SSTL
Loading	Addr, Clk: Tree routed Data: Point to point	Addr, Clk: Daisy-chain routed Data: Point to point
Termination	Addr: none Data: Dynamic on-die termination (ODT)	Addr: Fly-by Data: Dynamic ODT

DDR2 Loading



- **Addr, Cntl, Clocks for DDR2 DIMMs are tree routed**
- **Advantages:**
 - Equal delays to each memory device
- **Disadvantages:**
 - Large stub lengths induce delays and ringing
 - Termination for these signals must be added to host board

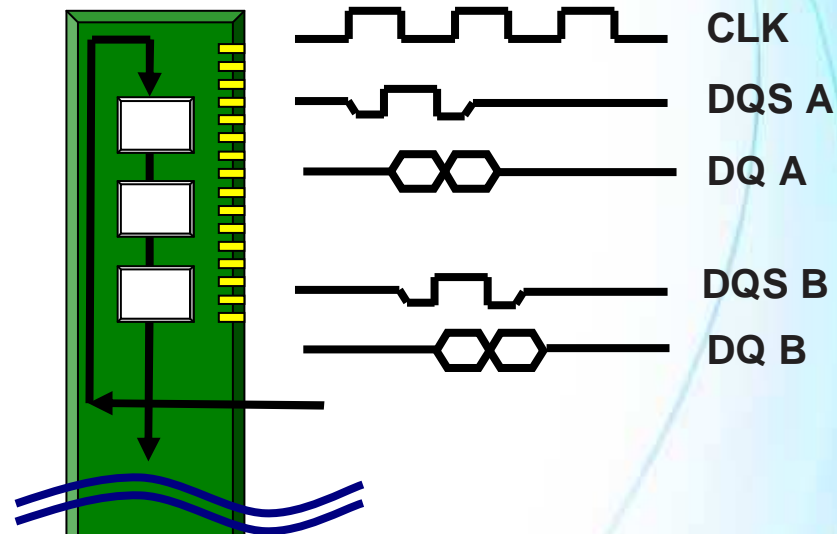
DDR3 Loading



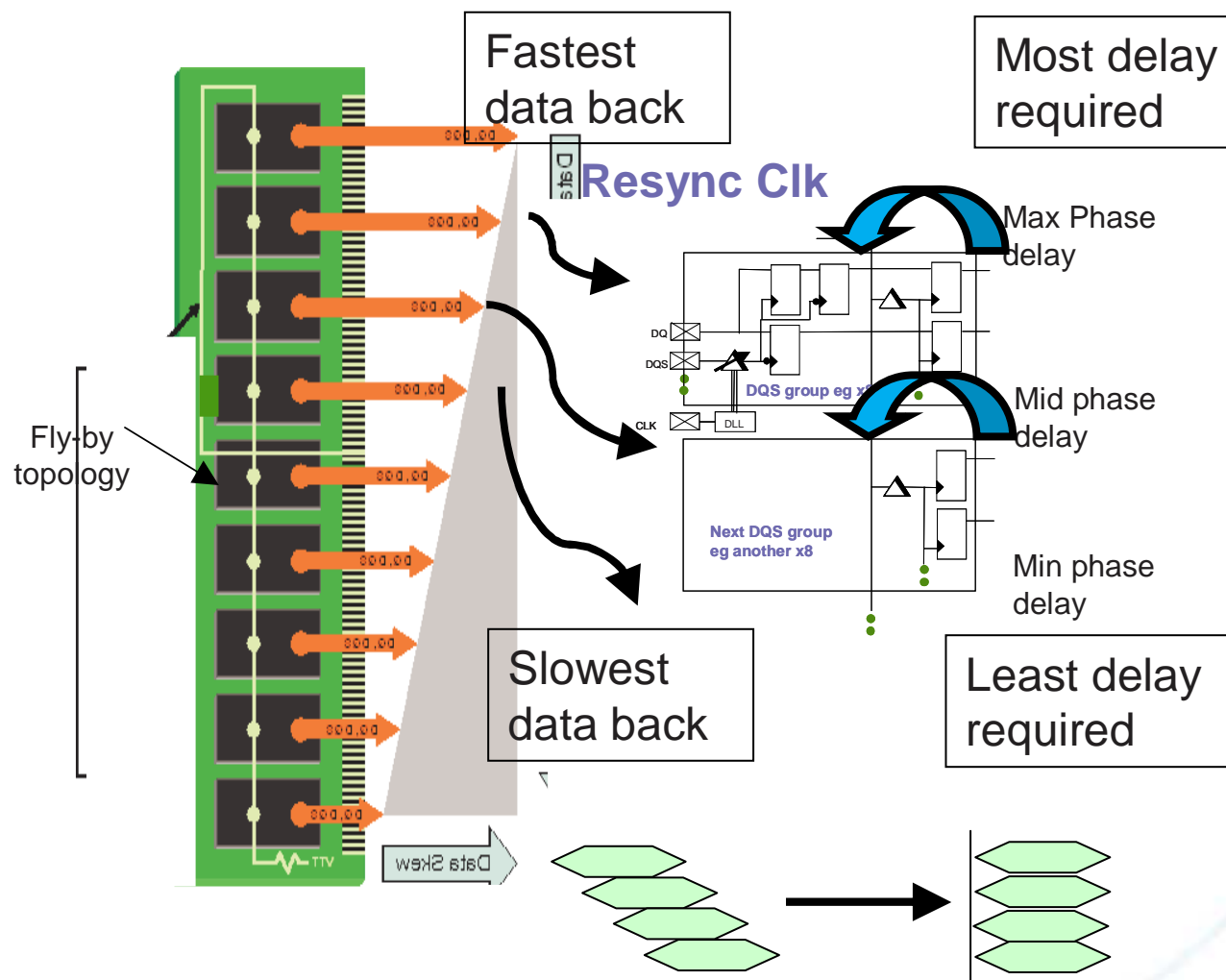
- **Addr, Cntl, Clocks for DDR3 DIMMS are daisy-chain routed**
- **Advantages:**
 - Reduction in number and length of stubs
 - Termination at end of line reduces noise
- **Disadvantages:**
 - Creates flight-time skew from one device to another

DDR3 – Read/Write Leveling

- DDR3 introduces skew to improve SI
 - Jedec-defined fly-by topology on Addr, Cntl and Clock signals
- Leveling
 - Compensates for skew between Addr, Cntl/Clock and DQS across DIMM
- Read leveling
 - Spread up to **TWO** clock cycles
- Write leveling
 - t_{DQSS} must be $\pm 0.25 t_{CK}$



Read Leveling for DDR3



Not I/O delays –
i.e., do not appear directly
in data path

Phase shifts of re-sync
clock position (PVT
compensated) effectively
block delay DQ data in
given DQS group

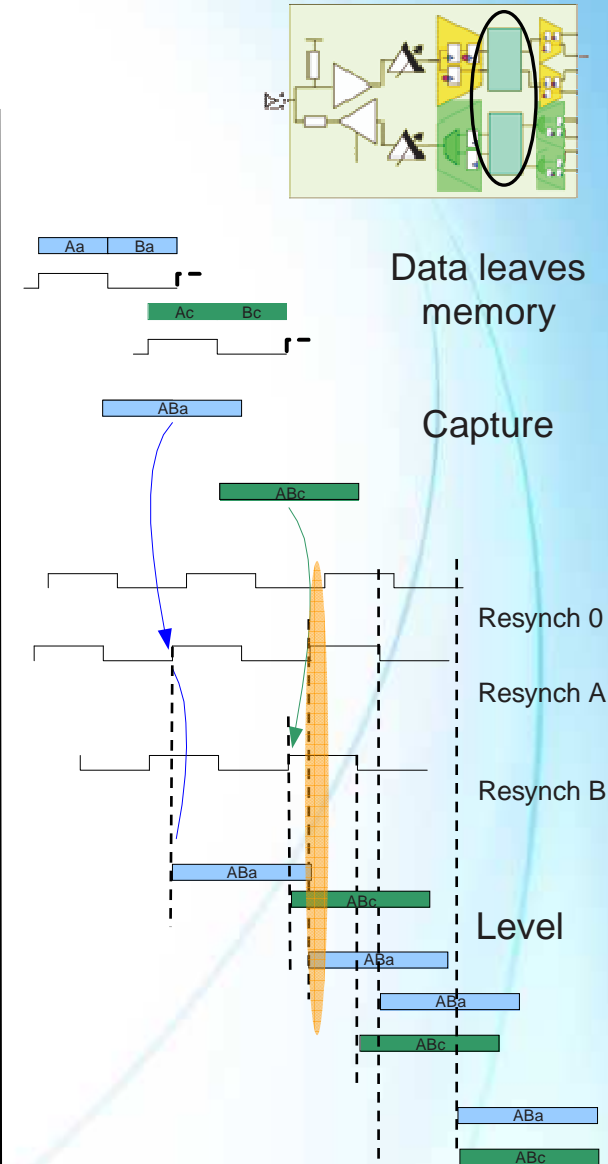
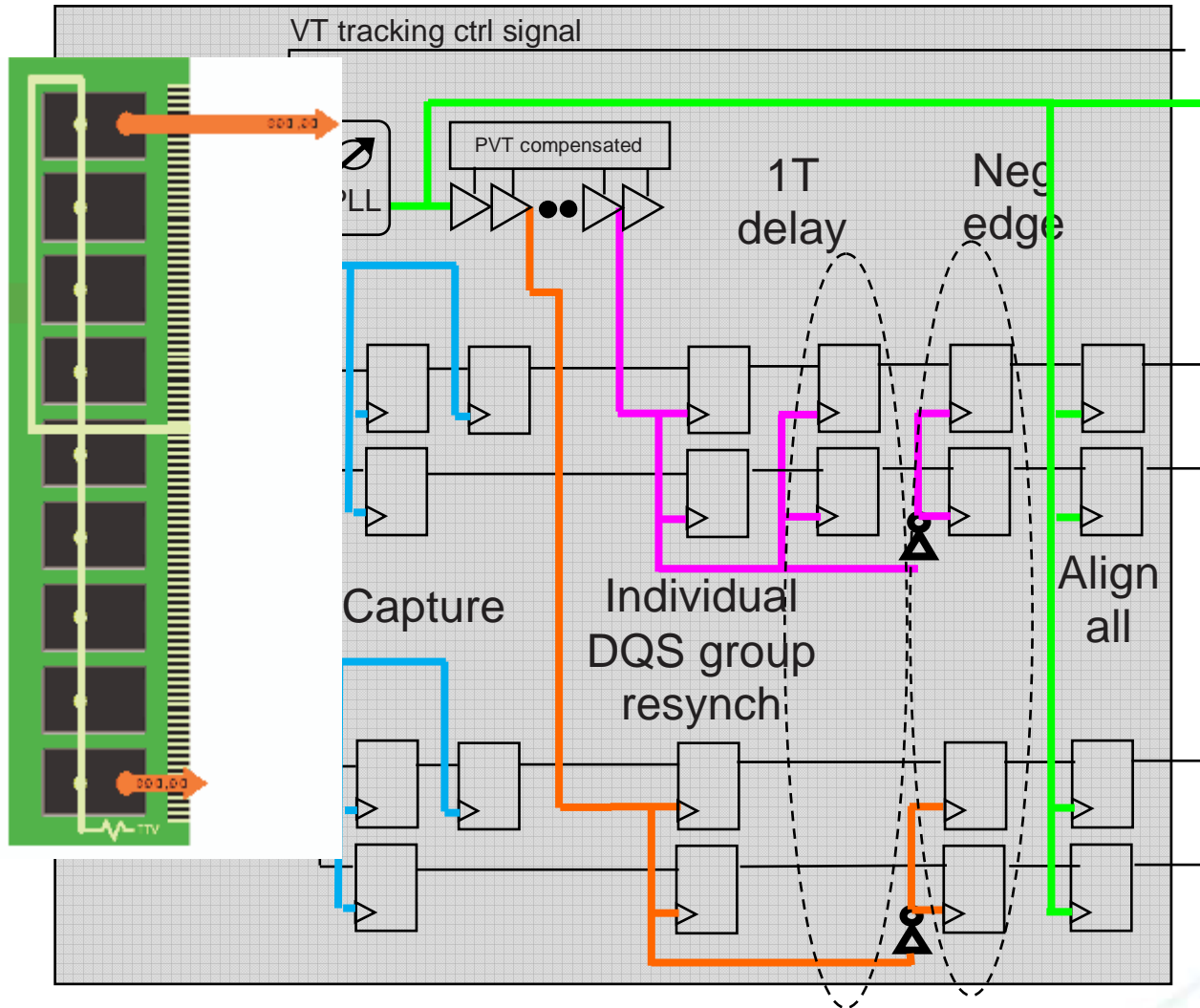
Each DQS group has own
phase shift

Consequently, all output
data across bus can be
aligned

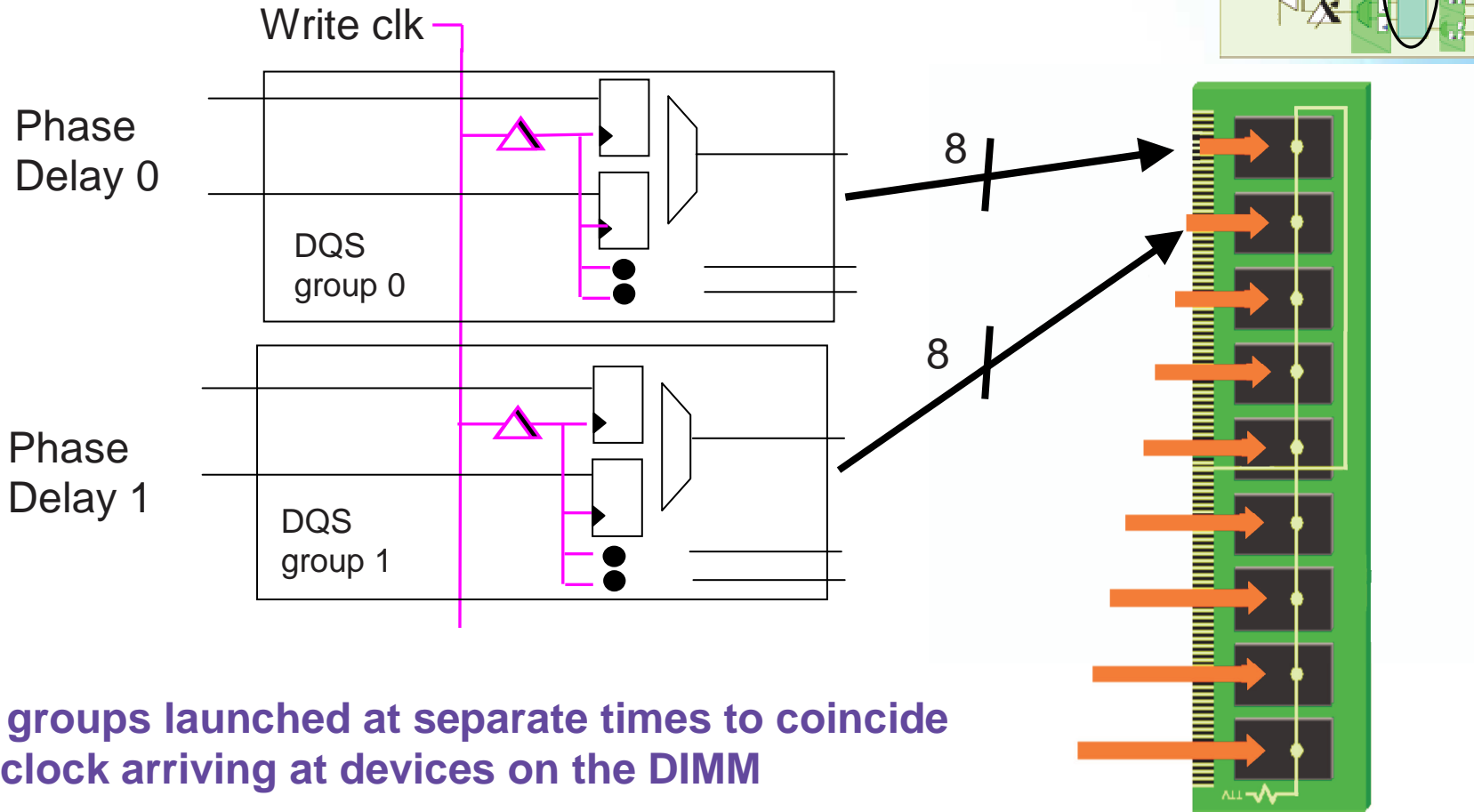
Individual DQ signals
within DQS group can be
aligned with I/O delay
elements

Stratix III DDR3 Read Levelling

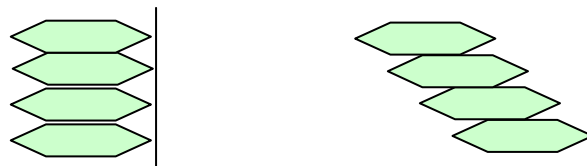
Stratix III I/O Block



Write Leveling Built Into I/O For DDR3



DQS groups launched at separate times to coincide with clock arriving at devices on the DIMM

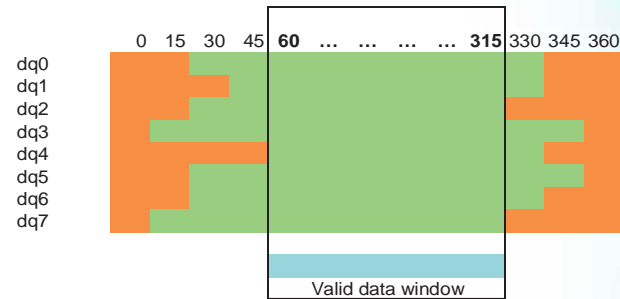


Some Techniques

Dynamic Calibration

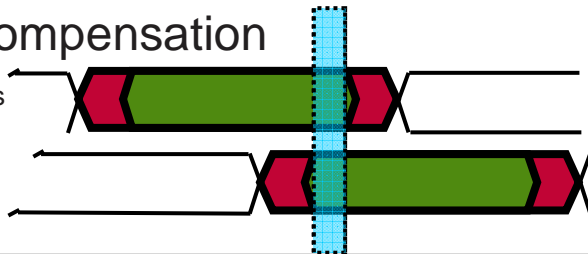
Without calibration: complex static timing analysis, narrow data valid window

With calibration: accurate strobe placement, wider data valid window

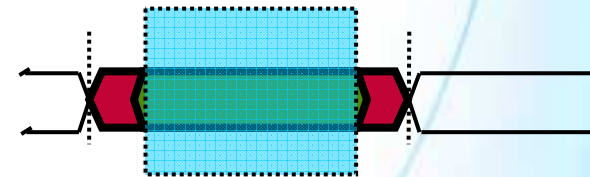


VT Compensation

Data shifts due to VT variations

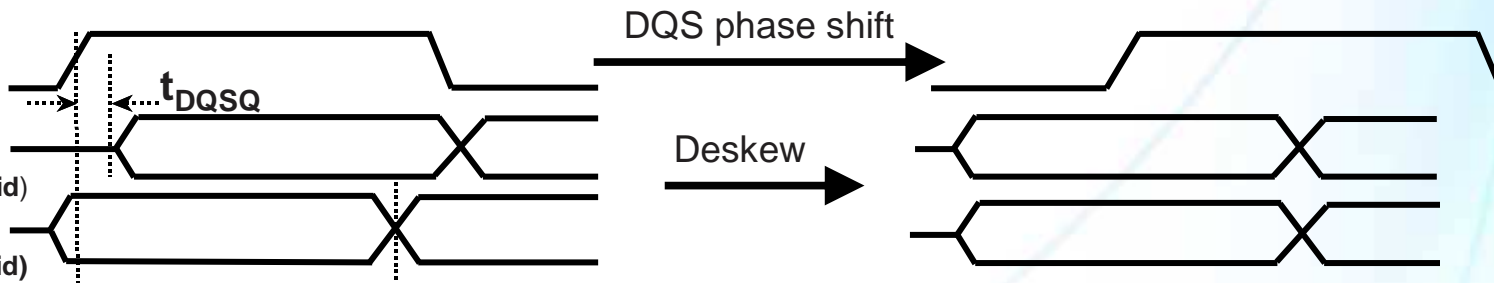


Voltage and temperature tracking



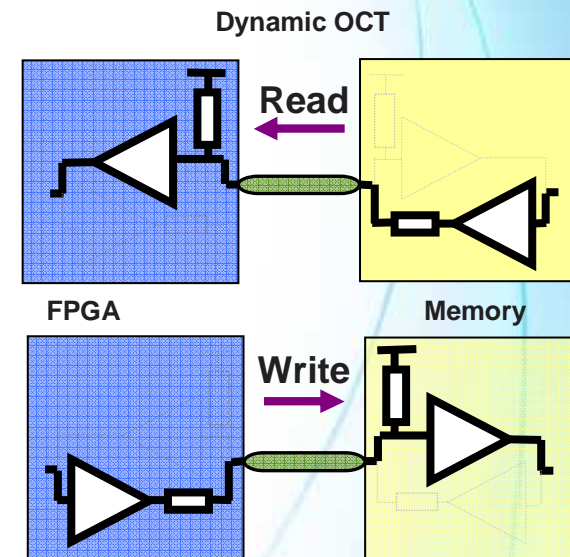
Deskew

DQ (Last Data Valid)
DQ (First Data Valid)



Termination (ODT)

- Dynamically turned ON & OFF parallel termination
 - **Significant power saving**
 - 1.6 watts over 72-bit DDR2 bus
 - **Proper line termination** for bidirectional busses
 - **Reduce costs**
 - Ease routing congestion
 - Put memories closer
 - Save external component cost



Implementing DDR3 With FPGA

■ FPGA needs:

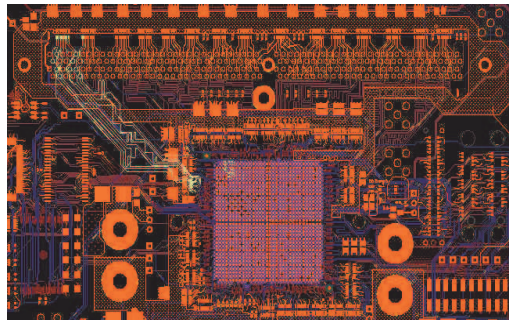
- Controller with read- and write-leveling capability
- Controller with flexibility to load variety of manufacturer's DIMMs
- Dynamic ODT capability
- Adjustable drive strength capability

■ Working example

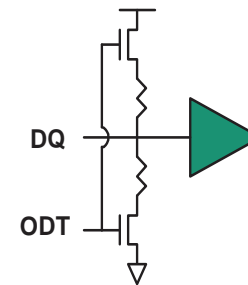
- 64-bit single-rank 533-MHz (1067-Mbps) DDR3 UDIMM

Methodology for Setup and Analysis of DDR3 Interfaces

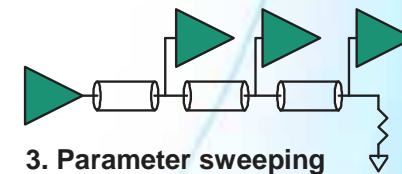
- Interface setup
- ODT setup
- Constraints development
- SI analysis
- Timing and noise margins determination



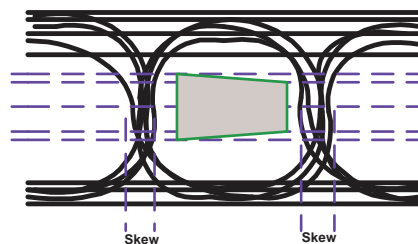
1. Interface setup



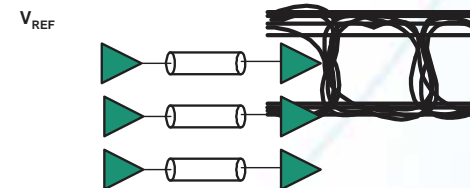
2. ODT setup



3. Parameter sweeping



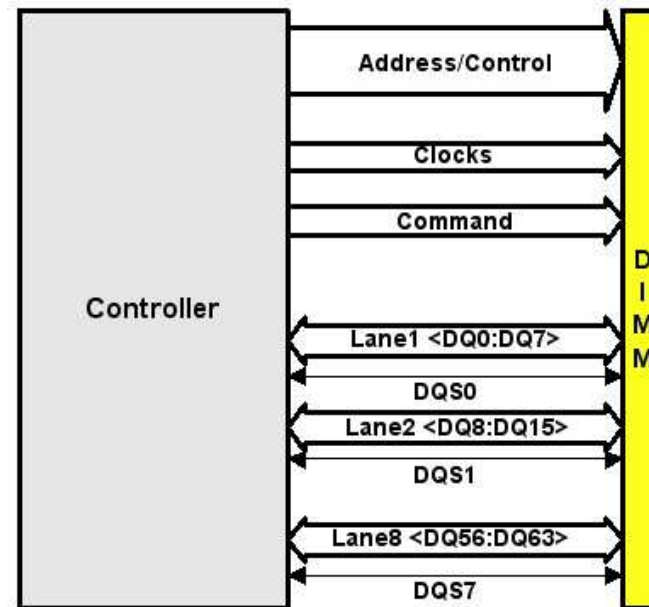
5. Measurements and slew rate derating



4. Reflection and xtalk analysis

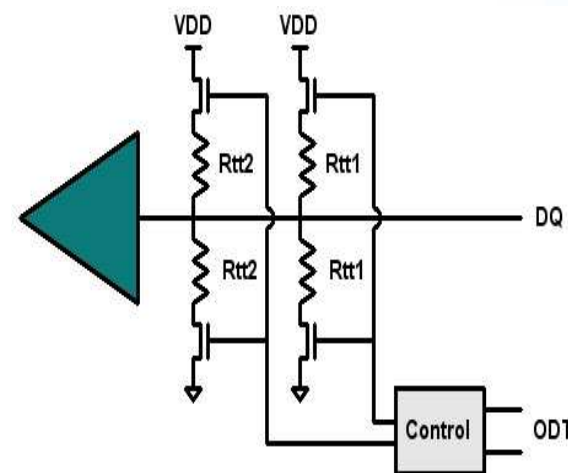
Interface Setup and Signal Associations

- Identify controller and DRAMs
- Define various bus objects (i.e., signal groups)
- Specify directionality of each bus
- Associate bus, lane, or bit with corresponding clock or strobe signal



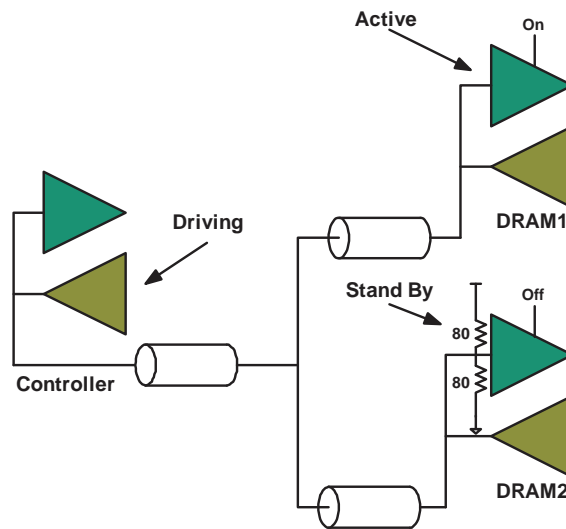
ODT Setup

- Programmable ODT for data signals to improve SI and reduce number of components on PCB
- DRAM ODT pin(s) used to turn terminations on/off
- ODT values differ when I/O is receiving or in standby mode
- Solution space exploration needed to determine optimal ODT values

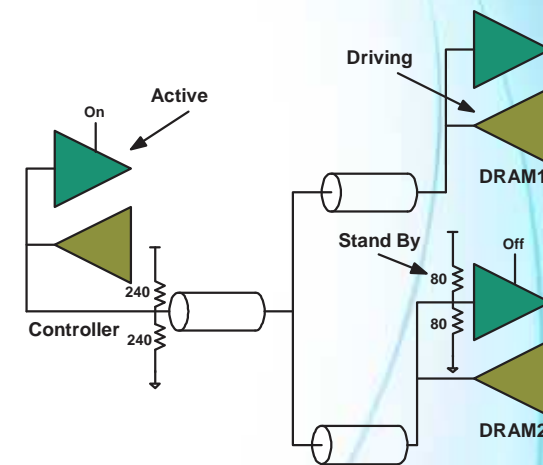


ODT Setup (cont.)

- ODT setup depends on read/write cycle as well as system configuration
- Use different IBIS I/O models for different settings
- IBIS model selector can be used to specify list of models to use
- Select buffer models to use when I/O is driving, receiving, or in standby mode



Memory Write



Memory Read

	Driver	Receiver	Standby Receivers
Controller	DRVR	RCVR_240	RCVR_240
DRAM1	DRVR	RCVR	ODT_80
DRAM2	DRVR	RCVR	ODT_80

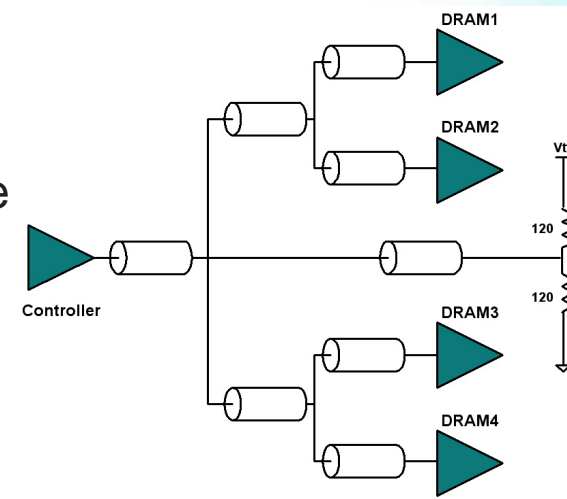
Solution Space Exploration

■ Pre-layout parameter sweep to:

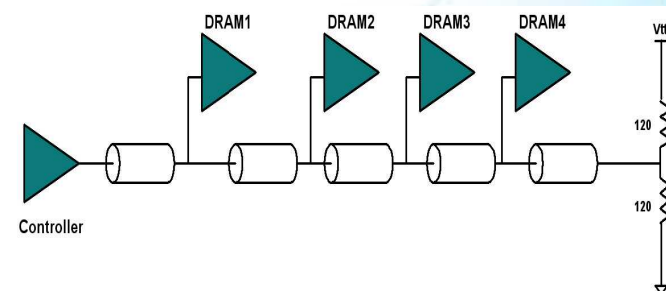
- Estimate stubs flight times to synchronize strobe with clock (read/write leveling), strobe with data, address with clock, etc.
- Determine trace parameters (e.g., width, spacing) and ODT values to improve SI
- Select I/Os with right strength and output impedance to drive bus

■ Based on that:

- Pass developed parameters to a constraint-driven router to layout system
- Shift strobe signals accordingly to support read/write leveling
- Assign I/O buffers and ODT values accordingly



DDR2 T-branch topology

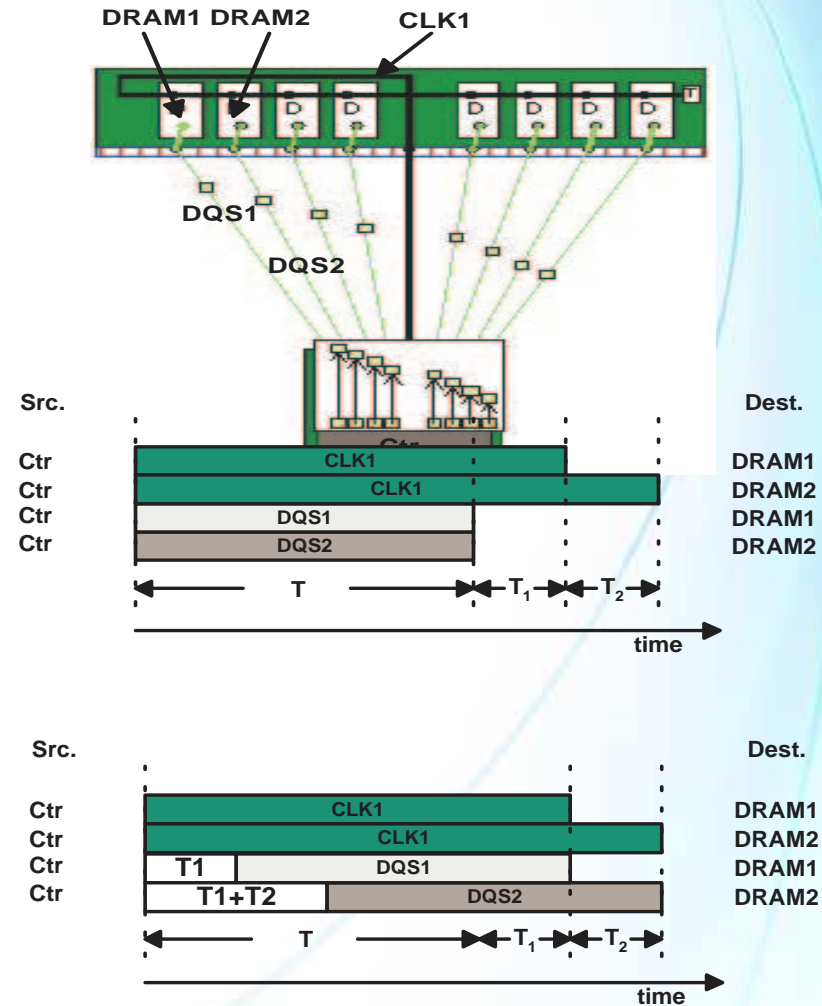


DDR3 fly-by topology

Solution Space Exploration (cont.)

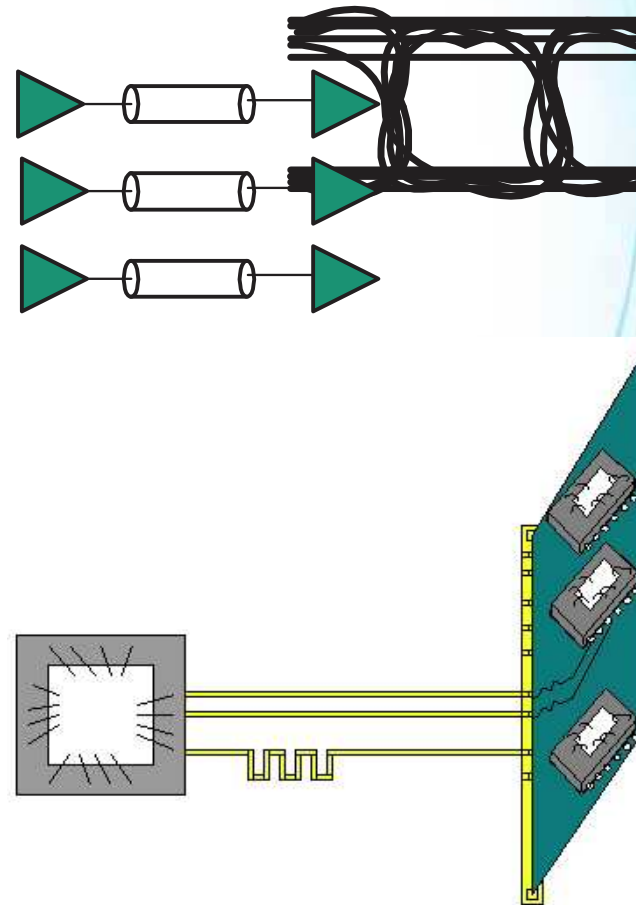
Write leveling as an example

- Based on a pre-route simulation:
 - DQS1 reaches DRAM1 at T
 - CLK1 reaches DRAM1 at $T+T_1$
 - DQS2 reaches DRAM2 at T
 - CLK1 reaches DRAM2 at $T+T_1+T_2$
- To model write leveling, we need to shift:
 - DQS1 by T_1
 - DQS2 by T_1+T_2



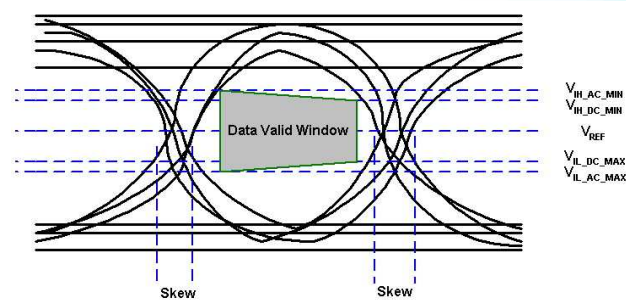
SI Analysis

- Automatically simulate all Tx/Rx combinations for all PVT variations and ODT configurations
- Perform both *Reflection* and *Comprehensive* (reflection, xtalk, and SSN) analysis
- Accurate models for passive structures (e.g., wire bonds, solder balls, traces, delay lines, connectors) are required to produce acceptable simulation results
- 3D-field solver, rather than quasi-static solver, is needed to generate passive models



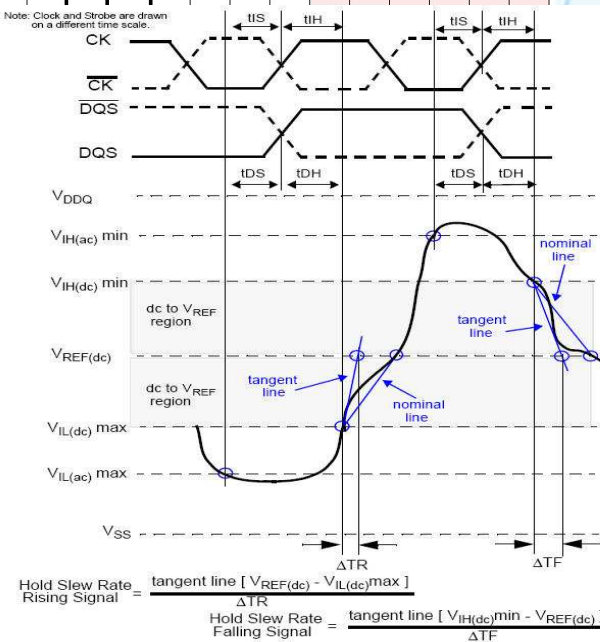
Measurements/Timing and Noise Margins

- Eye diagram display and measurements (e.g., jitter, height, width)
- Generate and display eye aperture
- Measure setup and hold times as well as flight times
- Measure data/strobe slew rate
- Slew rate derating
- Calculate noise margins and over/undershoot values
- Report timing and noise violations



		$\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based ¹																
		DQS, DQS# Differential Slew Rate																
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-	
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-	
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-	
	0.9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

NOTE:
1. Cell contents shaded in



Summary

- Discussed features and design challenges of DDR3 interfaces
- Presented methodology to tackle various DDR3 design challenges
- Proposed methodology is easy to follow and shortens design cycle

Questions?