Challenges in Implementing DDR3 Memory Interface on PCB Systems - A Methodology for Interfacing DDR3 SDRAM DIMM to an FPGA

Authors:
Phil Murray  Altera
Feras Al-Hawari  Cadence

Presenter:
Robert Blake  Altera
Roadmap

- Migration from DDR2 to DDR3
- DDR3 read/write leveling
- Methodology for setup and analysis of DDR3 interfaces
## Migration to DDR3

<table>
<thead>
<tr>
<th></th>
<th>DDR2 DIMM</th>
<th>DDR3 DIMM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Rate</strong></td>
<td>400-800 Mbps</td>
<td>800-1600 Mbps</td>
</tr>
<tr>
<td><strong>Voltage</strong></td>
<td>1.8V SSTL</td>
<td>1.5V SSTL</td>
</tr>
<tr>
<td><strong>Loading</strong></td>
<td>Addr, Clk: Tree routed</td>
<td>Addr, Clk: Daisy-chain routed</td>
</tr>
<tr>
<td></td>
<td>Data: Point to point</td>
<td>Data: Point to point</td>
</tr>
<tr>
<td><strong>Termination</strong></td>
<td>Addr: none</td>
<td>Addr: Fly-by</td>
</tr>
<tr>
<td></td>
<td>Data: Dynamic on-die termination (ODT)</td>
<td>Data: Dynamic ODT</td>
</tr>
</tbody>
</table>
**DDR2 Loading**

- **Addr, Cntl, Clocks for DDR2 DIMMs are tree routed**
- **Advantages:**
  - Equal delays to each memory device
- **Disadvantages:**
  - Large stub lengths induce delays and ringing
  - Termination for these signals must be added to host board
**DDR3 Loading**

- **Addr, Cntl, Clocks for DDR3 DIMMS are daisy-chain routed**
- **Advantages:**
  - Reduction in number and length of stubs
  - Termination at end of line reduces noise
- **Disadvantages:**
  - Creates flight-time skew from one device to another
DDR3 – Read/Write Leveling

- DDR3 introduces skew to improve SI
  - Jede-defined fly-by topology on Addr, Cntl and Clock signals

- Leveling
  - Compensates for skew between Addr, Cntl/Clock and DQS across DIMM

- Read leveling
  - Spread up to TWO clock cycles

- Write leveling
  - tDQSS must be ±0.25 tCK
Read Leveling for DDR3

Not I/O delays –
i.e., do not appear directly in data path

Phase shifts of re-sync clock position (PVT compensated) effectively block delay DQ data in given DQS group

Each DQS group has own phase shift

Consequently, all output data across bus can be aligned

Individual DQ signals within DQS group can be aligned with I/O delay elements
Stratix III DDR3 Read Levelling

Stratix III I/O Block

VT tracking ctrl signal

Capture

Individu al DQS group resynch

Align all

Level

PLL

PVT compensated

1T delay Neg edge

Capture Data leaves memory

Individual DQS group resynch

Resynch 0

Resynch A

Resynch B

Data leaves memory

Capture

Resynch 0

Resynch A

Resynch B

© 2008 Altera Corporation—Public

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation.
Write Leveling Built Into I/O For DDR3

DQS groups launched at separate times to coincide with clock arriving at devices on the DIMM.
Some Techniques

Dynamic Calibration

Without calibration: complex static timing analysis, narrow data valid window

With calibration: accurate strobe placement, wider data valid window

VT Compensation

Data shifts due to VT variations

Voltage and temperature tracking

Deskew

DQ (Last Data Valid)

DQ (First Data Valid)

DQS phase shift

Deskew
Termination (ODT)

- Dynamically turned ON & OFF parallel termination
  - **Significant power saving**
    - 1.6 watts over 72-bit DDR2 bus
  - **Proper line termination** for bidirectional busses
  - **Reduce costs**
    - Ease routing congestion
    - Put memories closer
    - Save external component cost
Implementing DDR3 With FPGA

- FPGA needs:
  - Controller with read- and write-leveling capability
  - Controller with flexibility to load variety of manufacturer’s DIMMs
  - Dynamic ODT capability
  - Adjustable drive strength capability

- Working example
  - 64-bit single-rank 533-MHz (1067-Mbps) DDR3 UDIMM
Methodology for Setup and Analysis of DDR3 Interfaces

- Interface setup
- ODT setup
- Constraints development
- SI analysis
- Timing and noise margins determination

1. Interface setup
2. ODT setup
3. Parameter sweeping
4. Reflection and xtalk analysis
5. Measurements and slew rate derating
Interface Setup and Signal Associations

- Identify controller and DRAMs
- Define various bus objects (i.e., signal groups)
- Specify directionality of each bus
- Associate bus, lane, or bit with corresponding clock or strobe signal
ODT Setup

- Programmable ODT for data signals to improve SI and reduce number of components on PCB
- DRAM ODT pin(s) used to turn terminations on/off
- ODT values differ when I/O is receiving or in standby mode
- Solution space exploration needed to determine optimal ODT values
ODT Setup (cont.)

- ODT setup depends on read/write cycle as well as system configuration
- Use different IBIS I/O models for different settings
- IBIS model selector can be used to specify list of models to use
- Select buffer models to use when I/O is driving, receiving, or in standby mode

<table>
<thead>
<tr>
<th></th>
<th>Driver</th>
<th>Receiver</th>
<th>Standby Receivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller</td>
<td>DRVR</td>
<td>RCVR_240</td>
<td>RCVR_240</td>
</tr>
<tr>
<td>DRAM1</td>
<td>DRVR</td>
<td>RCVR</td>
<td>ODT_80</td>
</tr>
<tr>
<td>DRAM2</td>
<td>DRVR</td>
<td>RCVR</td>
<td>ODT_80</td>
</tr>
</tbody>
</table>
Solution Space Exploration

- **Pre-layout parameter sweep to:**
  - Estimate stubs flight times to synchronize strobe with clock (read/write leveling), strobe with data, address with clock, etc.
  - Determine trace parameters (e.g., width, spacing) and ODT values to improve SI
  - Select I/Os with right strength and output impedance to drive bus

- **Based on that:**
  - Pass developed parameters to a constraint-driven router to layout system
  - Shift strobe signals accordingly to support read/write leveling
  - Assign I/O buffers and ODT values accordingly
Solution Space Exploration (cont.)
Write leveling as an example

- Based on a pre-route simulation:
  - DQS1 reaches DRAM1 at T
  - CLK1 reaches DRAM1 at T+T1
  - DQS2 reaches DRAM2 at T
  - CLK1 reaches DRAM2 at T+T1+T2

- To model write leveling, we need to shift:
  - DQS1 by T1
  - DQS2 by T1+T2
SI Analysis

- Automatically simulate all Tx/Rx combinations for all PVT variations and ODT configurations
- Perform both Reflection and Comprehensive (reflection, xtalk, and SSN) analysis
- Accurate models for passive structures (e.g., wire bonds, solder balls, traces, delay lines, connectors) are required to produce acceptable simulation results
- 3D-field solver, rather than quasi-static solver, is needed to generate passive models
Measurements/Timing and Noise Margins

- Eye diagram display and measurements (e.g., jitter, height, width)
- Generate and display eye aperture
- Measure setup and hold times as well as flight times
- Measure data/strobe slew rate
- Slew rate derating
- Calculate noise margins and over/undershoot values
- Report timing and noise violations
Summary

- Discussed features and design challenges of DDR3 interfaces
- Presented methodology to tackle various DDR3 design challenges
- Proposed methodology is easy to follow and shortens design cycle
Questions?