



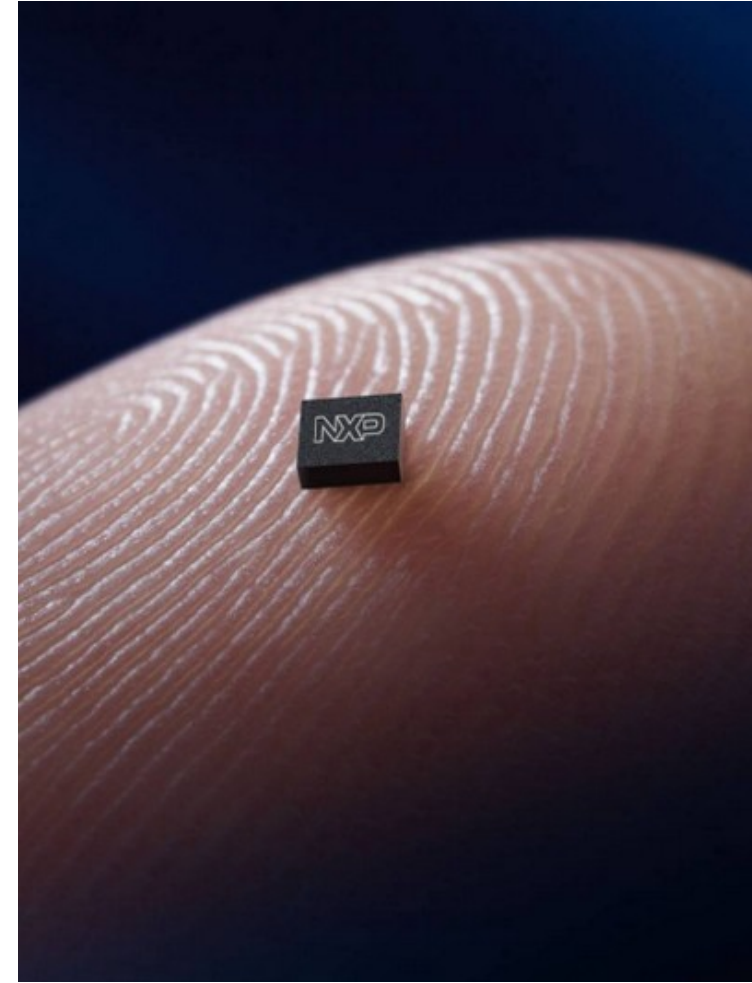
Experiences from a CPF enabled low power design from RTL-GDS2

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Digital IC design #2.7
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Outline

- ▶ NXP Semiconductors
- ▶ Why power management?
- ▶ Impact of power reduction techniques
- ▶ Experiences implementing a MSV SoC
- ▶ Conclusions



NXP Semiconductors

- ▶ Spin-out of Royal Philips Electronics' Semiconductor Division
- ▶ Top-10 global supplier with Sales of \$ 6.32 Bln (2007)
- ▶ 37,000 employees / 7,500 engineers
- ▶ Investing \$1.4 Bln in R&D annually
- ▶ 25,000+ patents
- ▶ More than 26 R&D centers in 12 countries
- ▶ Participation in over 100 standardization bodies and consortia



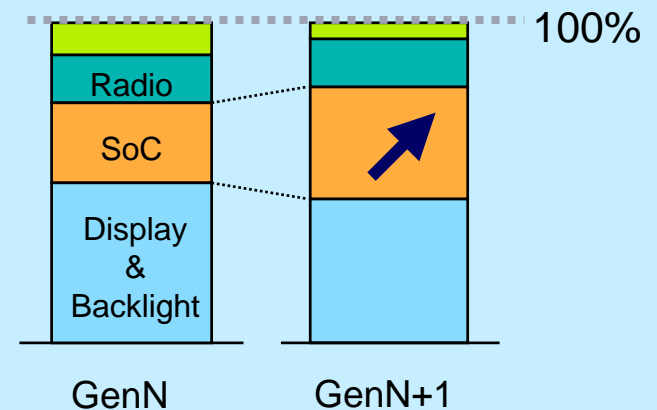
Why Power Management?



- ▶ Battery Life
- ▶ Play Time
- ▶ Green Initiatives
- ▶ Money

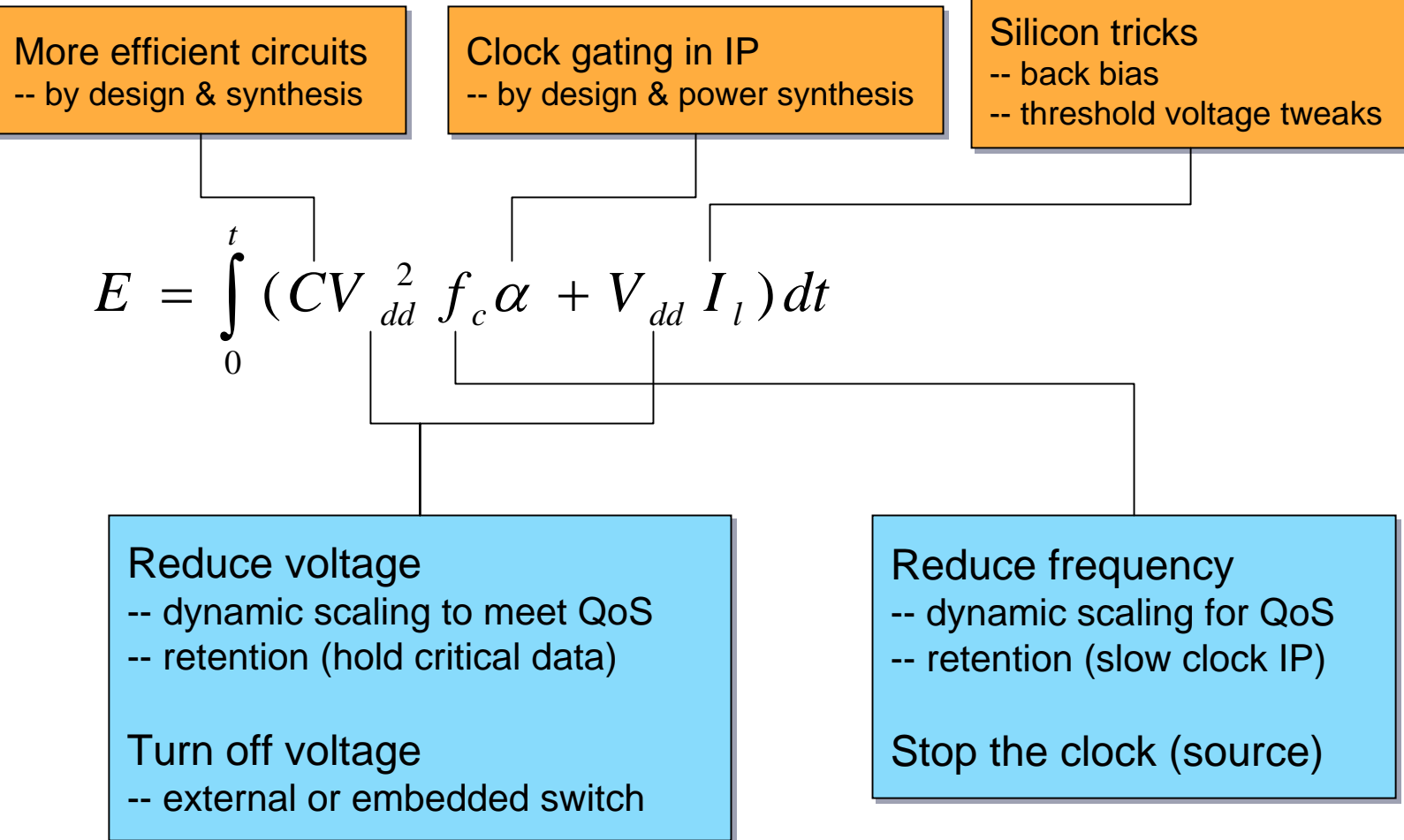
▶ Why SoC power management?

- ▶ SoC power trends are concerning
- ▶ SoC power consumption is rapidly increasing relative to rest of system
 - ▶ On par with radio interface and approaching the display!



Impact of Power Reduction Techniques

Power Reduction Techniques overview



Impact of Power Reduction Techniques

Impact overview

Power Reduction Technique	Power Benefit	Timing Penalty	Area Penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Multi-Vt Optimization	Medium	Little	Little	Low	Low	None	Low
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi-Supply Voltage	Large	Some	Little	High	Medium	Low	Medium
Power Shutoff	Huge	Some	Some	High	High	High	High
Dynamic and Adaptive Voltage Frequency Scaling	Large	Some	Some	High	High	High	High
Substrate Biasing	Large	Some	Some	Medium	None	None	High

[source: Cadence]

Impact of Power Reduction Techniques

Problem statement

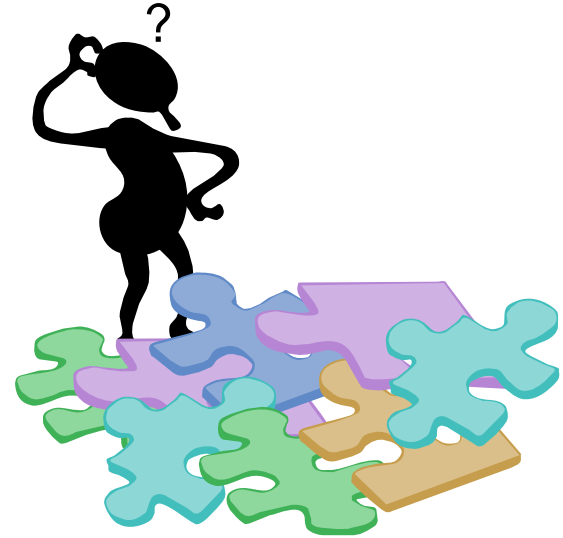
- ▶ Power and ground nets are now becoming functional nets.
- ▶ Being able to verify the power down modes, retention, recovery at power-on, etc. in the context of RTL simulation is becoming mandatory.
- ▶ Voltage islands increase the complexity and throughput time of implementation.
- ▶ No formal repository (format or language) for capturing the low power constraints for a design.
 - Many implementation tools now need to understand this information.
 - Today recaptured as many times as required. Recipe for disaster.
- ▶ Need to converge on a design specification for low power.
 - Today two standards are there: CPF/UPF.
 - An improved standard is under work: IEEEp1801.



Experiences implementing a MSV SoC

SoC integration becomes more complex

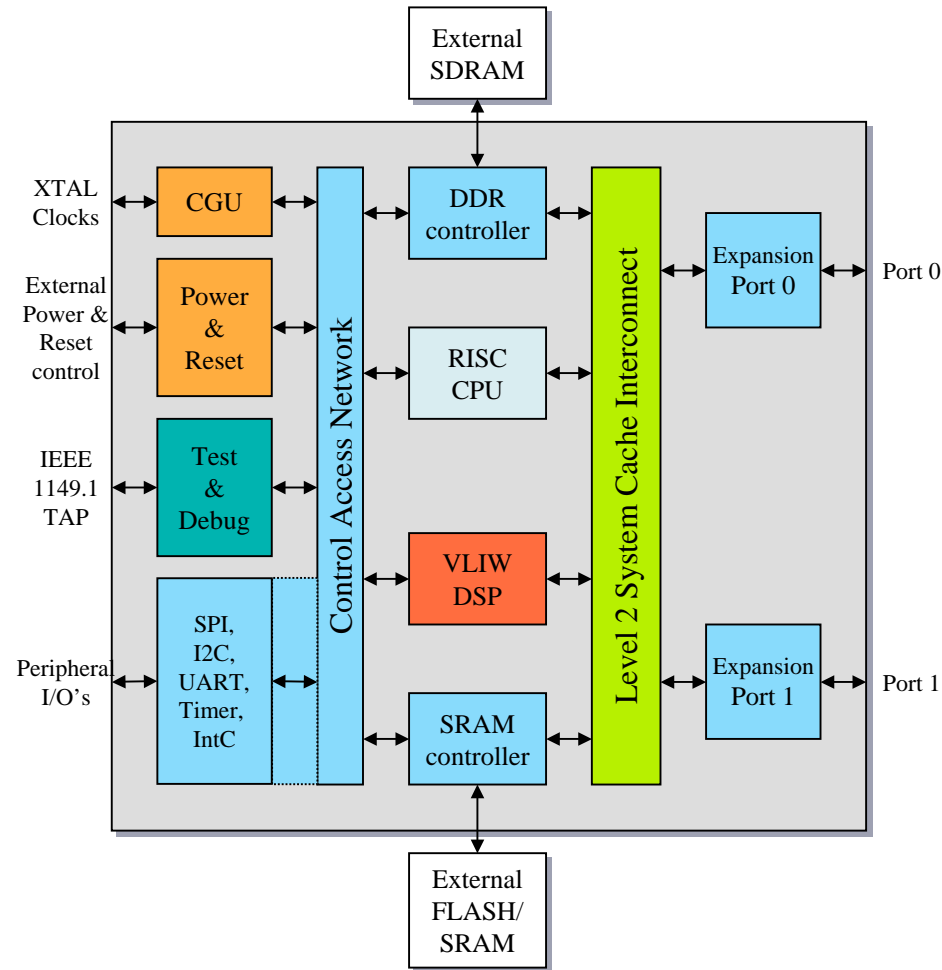
- ▶ Design-in and Verification
- ▶ Static Timing Analysis (STA)
- ▶ Signal distribution
- ▶ Design For Test (DFT)
- ▶ Hierarchy
- ▶ Power distribution
- ▶ ...



The total problem is more than the sum of its parts!

Experiences implementing a MSV SoC

Some Key Architectural Components

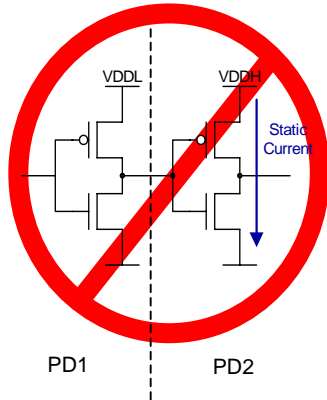


- ▶ The SoC consists of 11 islands.
- ▶ 3 voltage scalable logic sections.
- ▶ 3 on-chip switch able domains.
- ▶ 5 off-chip switch able domains.
- ▶ 5 off-chip separate switch able pad ring sections.
- ▶ The 3 major power consumers (RISC CPU, VLIW DSP and L2 System Cache) are controlled using AVS.

Experiences implementing a MSV SoC

New rules

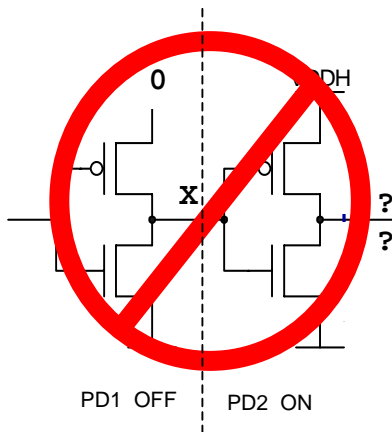
- ▶ With Multiple Supplies (V_{DDL} , V_{DDH})



1. Cannot directly connect V_{DDL} and V_{DDH} cells
 - Output of V_{DDL} gate can't be raised higher than V_{DDL}
 - When connected to V_{DDH} gate, PMOS will never be completely cut-off → Static Leakage Current,

Rule: Use Level Shifters

- ▶ For power switching



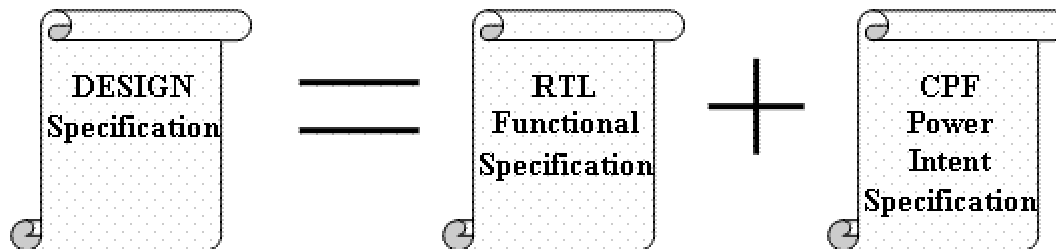
2. Cannot directly connect output of a powered down block.
 - Can propagate unwanted data in the logic driven
 - Floating input will potentially generate short circuit current.

Rule: Use clamps to force specific Inactive state on inputs driven by power down logic

Experiences implementing a MSV SoC

A placeholder mechanism for Power intent specification

- ▶ Power and Ground traditionally defined and implemented in the layout phase as they had no functional impact.
- ▶ Power gating is making PG nets partly functional as the behavior of the device depends on their state (clamping value) and level (performance).
- ▶ RTL does not have explicit representation of these nets, nor do the logic views for the leaf cells.

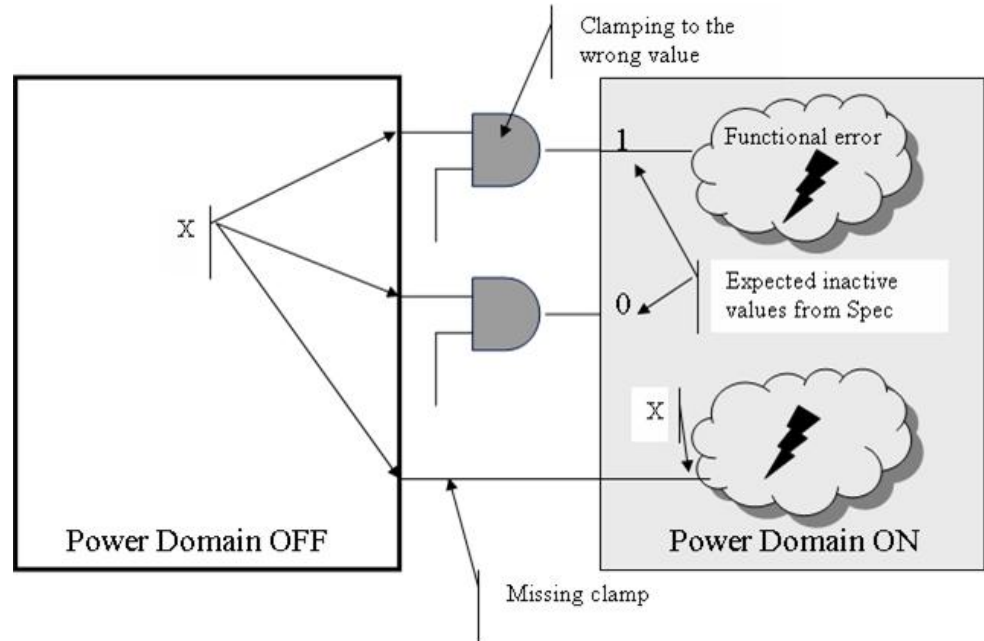


Experiences implementing a MSV SoC

The added value of CPF in verification (1/2)

How do we validate?

- 1) clamp control
- 2) right clamp value
- 3) missing clamps
- 4) re-initialize after powerdown



- ▶ Simulation of power switching can now be done in RTL
 - Power-up, -down simulations typically are slow
 - RTL simulations are much faster than netlist simulations
 - This really is a must (see next example...)

Experiences implementing a MSV SoC

Hierarchical usage (1/2)

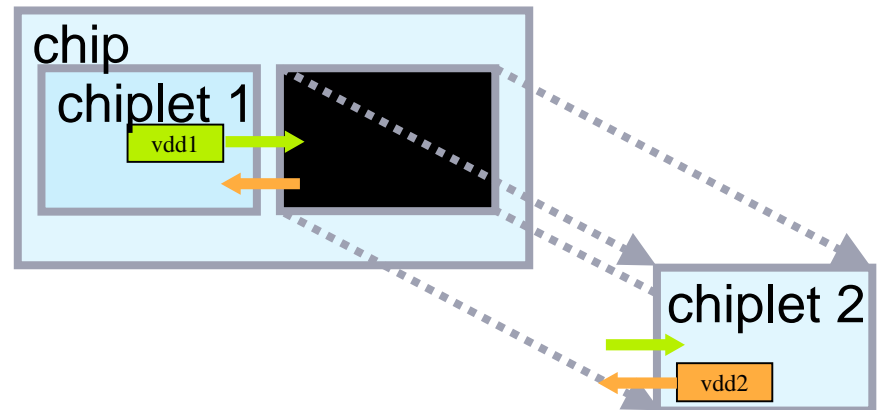
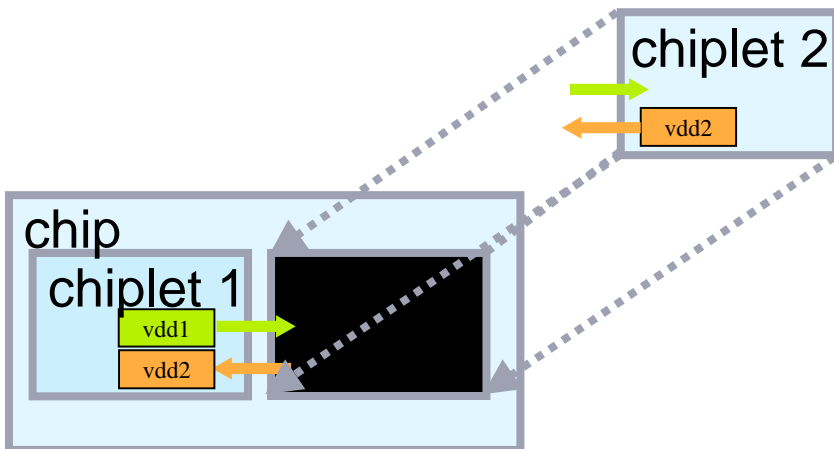
Tools and Format must support hierarchical Power Intent description

Bottom-up: power intent should be transported to top-level:

- It should be reusable for the integration of this IP.
- Should automatically be derived during the IP implementation.

Top-down: power intent should be transported to chiplets:

- From Chip-level power intent, chiplets should have their power constraints derived during partitioning.



Experiences implementing a MSV SoC

Hierarchical usage (2/2)

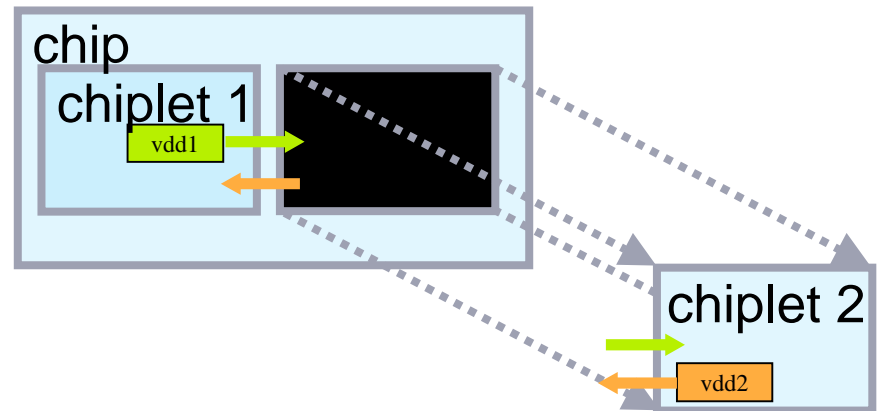
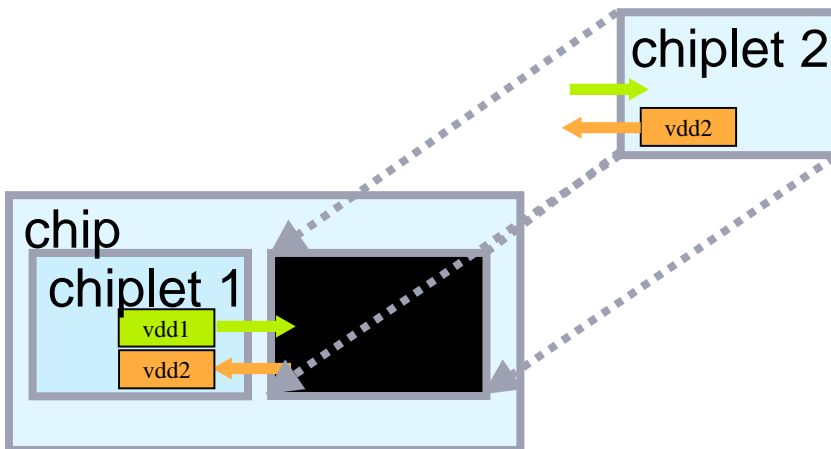
Current limitations:

Bottom-up:

- CPF cannot source another CPF when `create_power_domain` is used

Top-down:

- Only encounter supports the partitioning of CPF (>7.1)
- How to handle hierarchical synthesis?



Experiences implementing a MSV SoC

The added value of CPF in STA (1/2)

- ▶ With Dynamic Voltage Frequency Scaling, an “active” block will mean a range of operating voltages.
- ▶ Which STA use-cases are needed to guarantee working silicon?
- ▶ CPF helps, by allowing the user to specify the different modes and attach separate timing models and constraints:

```
create_power_mode -name mp3 -domain_conditions { \  
    RISC_VDD_domain@wc_0v8 \  
    L2_VDD_domain@wc_1v0 }  
  
update_power_mode -name mp3 -sdc_files $sdc
```

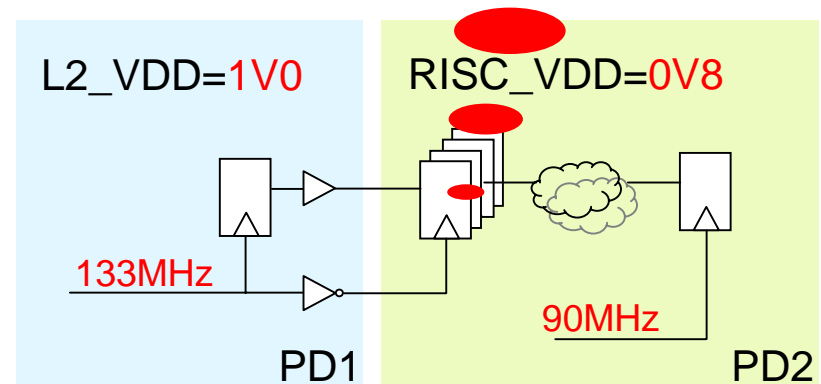
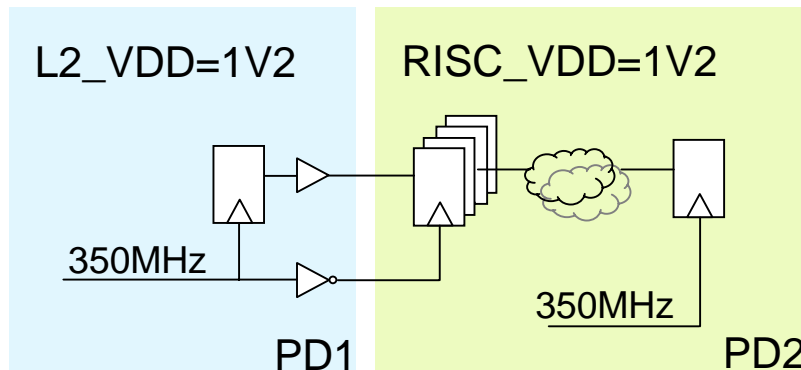
- ▶ Multi-mode, Multi-corner & Multi-voltage optimization+STA are a must (see next example...)

Experiences implementing a MSV SoC

The added value of CPF in STA (2/2)

- The below example shows the need to validate setup at lower voltages

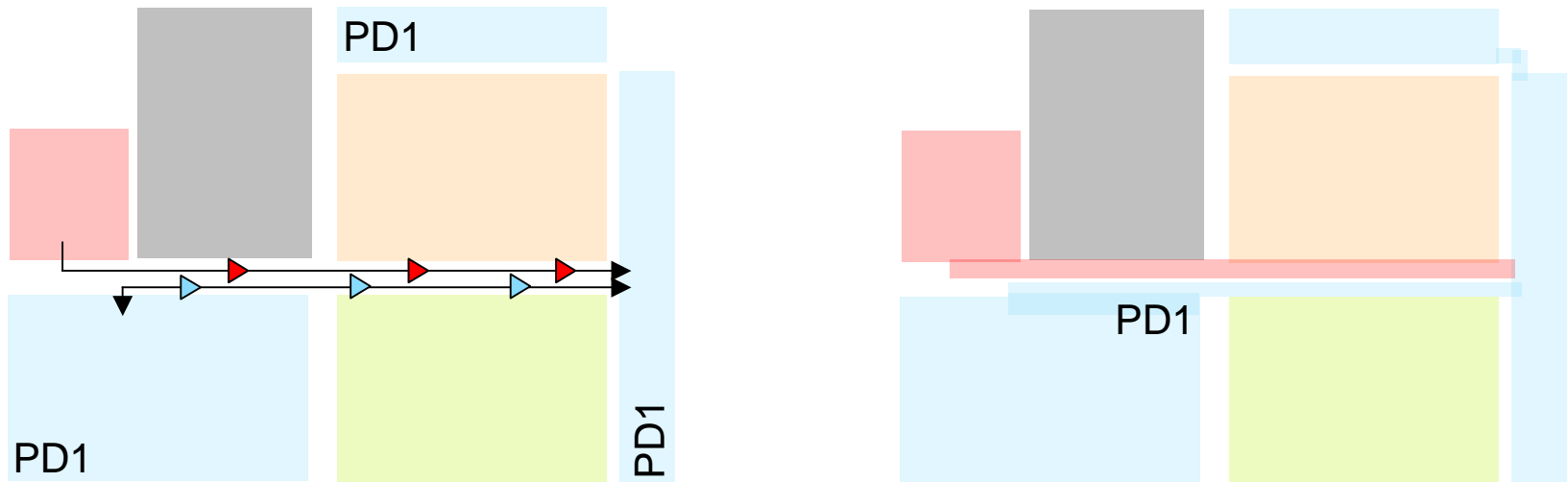
Mode	RISC CPU	L2 Memory network
Gaming	350MHz 1V2	350MHz 1V2
mp3	90MHz 0V8	133MHz 1V0
Paging	60MHz 0V6	-



Experiences implementing a MSV SoC

MSV Repeating (1/2)

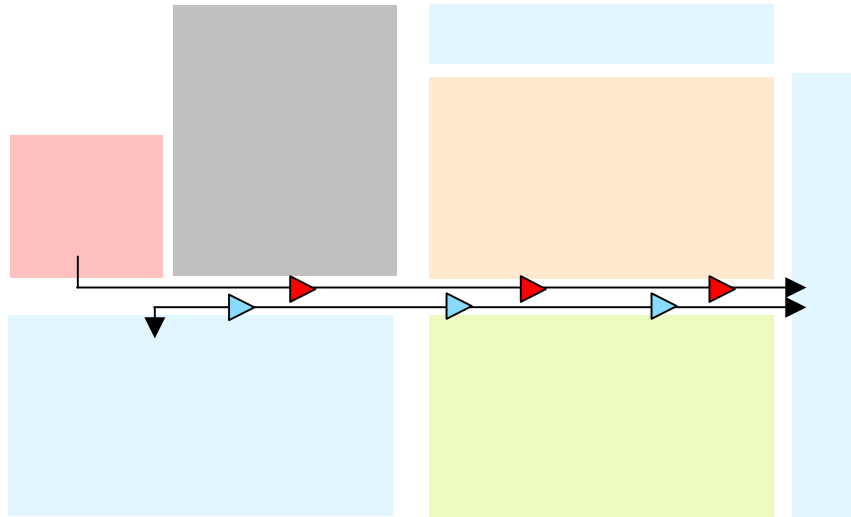
- ▶ Encounter currently is not supporting disjoint areas for same power domain (being enhanced in 7.1 to support this)
 - But with some creativity, one could get around
- ▶ On integration level repeaters need to be inserted
 - Without breaking the power intent



Experiences implementing a MSV SoC

MSV Repeating (2/2)

- ▶ How to create regions, and force repeatering through these?
(Work in progress for FE)
- ▶ Where to place the buffers in the logic hierarchy?
(Separate hierarchy? Sending hierarchy?)



Experiences implementing a MSV SoC

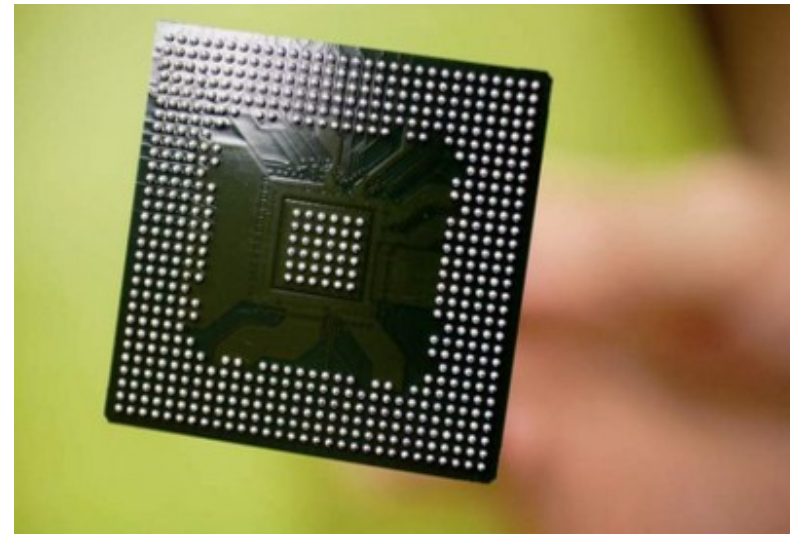
We have come a long way...

- ▶ Started as one of the first users of CPF in Q3 2006
- ▶ CPF was for the tools
 - a different language for already existing commands
 - a totally new concept
- ▶ CPF went from a 'plug-in' into a full-supported feature
- ▶ **Warning:** when using only 1 CPF file for implementation & verification
 - If not everything is simulated, best to make a separate CPF for verification inside conformal LP. Otherwise wrong coding, or wrong spec interpretation will simply ripple through the whole design!

Silicon is back, and fully functional, including all power features!

Conclusion

- ▶ Current state of art low power design has **significant** impact on **all** design flow stages
- ▶ Turnaround time has improved
 - Low power design is moving from hand crafting to automation
 - Tools now go beyond providing the basic low level hooks
- ▶ One Power Format as a standard, a big step in the right direction
 - Future improvements needed:
 - Hierarchical support for CPF
 - Multi-voltage repeatering inside encounter
 - Multi Mode Multi Corner support
- ▶ The risk of making a large, complex, Multi Supply Voltage design has become acceptable using CPF



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