



# A novel multi-clock generator: eliminating multiple PLLs

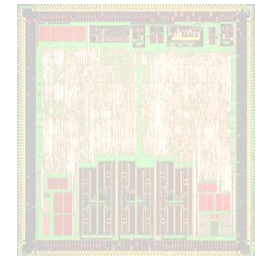
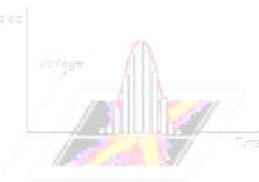
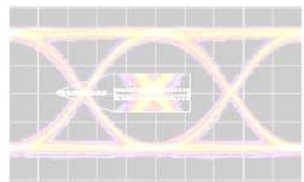
Solving multi-core frequency and  
power management issues

James Brodrick CTO, Toric Ltd

CDNLive! EMEA 2008, Munich, 29<sup>th</sup> April 2008

# Agenda

- IC power consumption trends
- Clock generation & power
- Scalability of clock generation methods
- Toric Multi-Clock Generator
- Anti Jitter Cell technology
- Work on simulation methods: Virtuoso



# Processors demand power



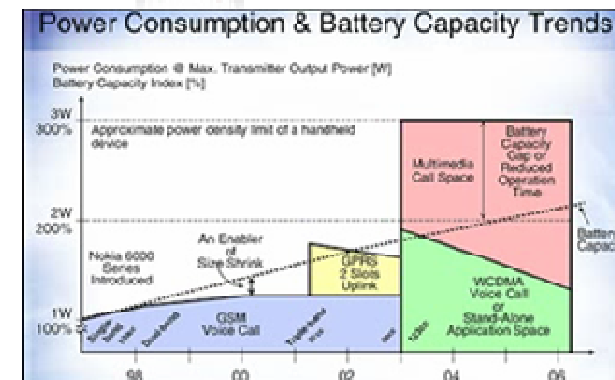
- IT infrastructure:
  - massive energy requirement
    - power \$ > equipment
    - \$3.3Bn



- battery capacity
  - being outstripped by load
    - handset capacity peaked in 2004
    - Nokia Navigator: battery life = 1 day

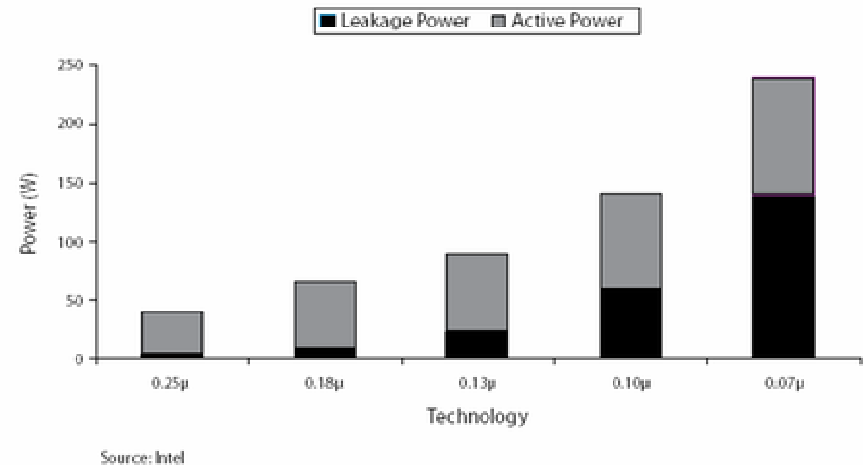


- power is limiting new designs:
  - issues with
    - reliability
    - yield

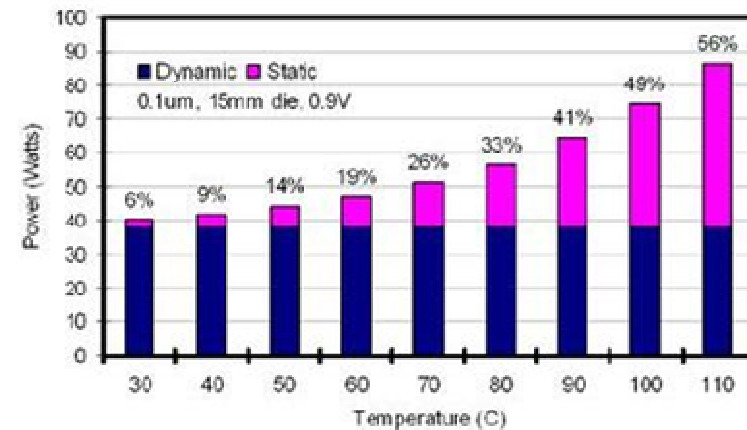


# Chip power consumption

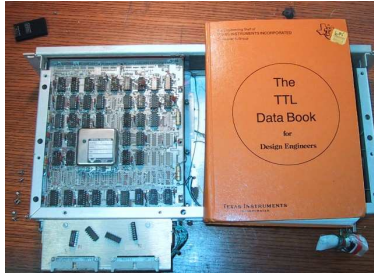
- active power is under control  
... but not leakage power



- The hotter it gets, the more it leaks
  - 0.64W/sq mm
- industry response:
  - *materials*: low-K, etc
  - *methods*: UPF, tools



# IC power: why does clocking come in?



70's – 80's: leave it on



2008: billion-transistor meltdown?

- clocking is power-hungry
- dynamic voltage/frequency scaling (DVFS)
- tight power control requires low latency:
  - Rapid power-up
  - Rapid clock run-up
- long clock run-up = long latency = lower performance

```
Codec_power_up();  
Status = frame_decode();  
Codec_power_down;
```

# Multicore and/or multi-clock domain SoCs

- scaling out, not up

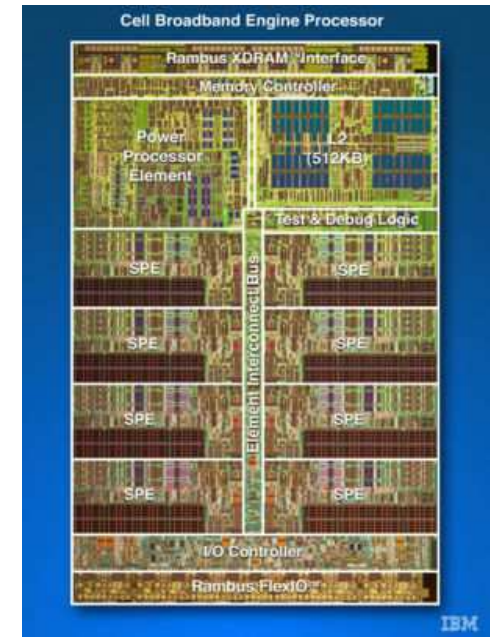
gives:

- ✓ lower power consumption
- ✓ lower clock frequencies
- ✓ higher performance (GFLOPS)

- however, there are issues

(ref. MultiCore Expo)

- ☹️ designing systems and developing software
- ☹️ **frequency control and power management**
- ☹️ interconnectivity and memory access



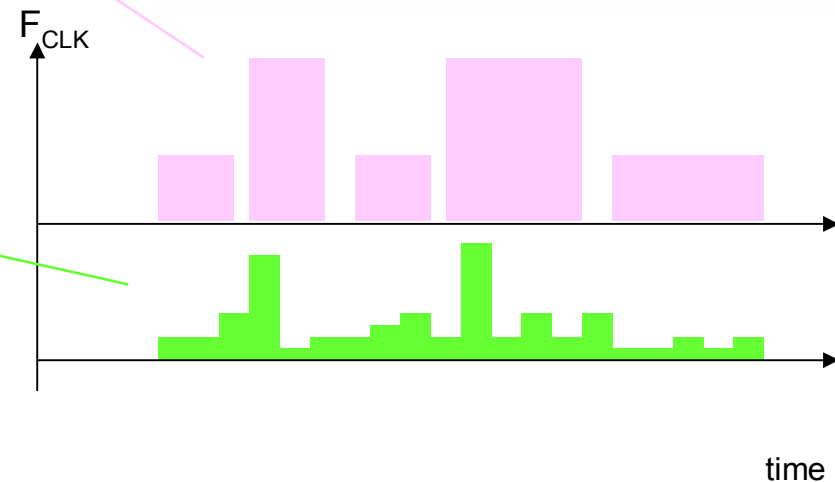
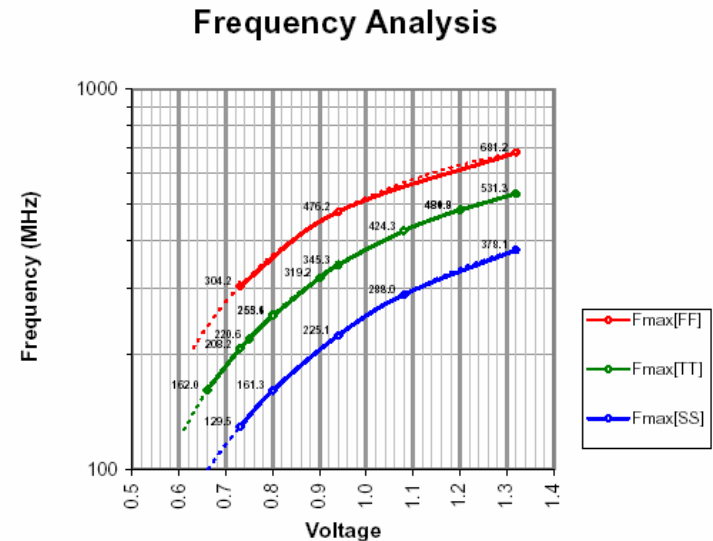
# Effective DVFS: power management

## Coarse-grain

- eg Intel SpeedStep, AMD CoolINQuiet, PowerNow
- performance (P) states, throttling (T) states
- latency between states due to run-up time

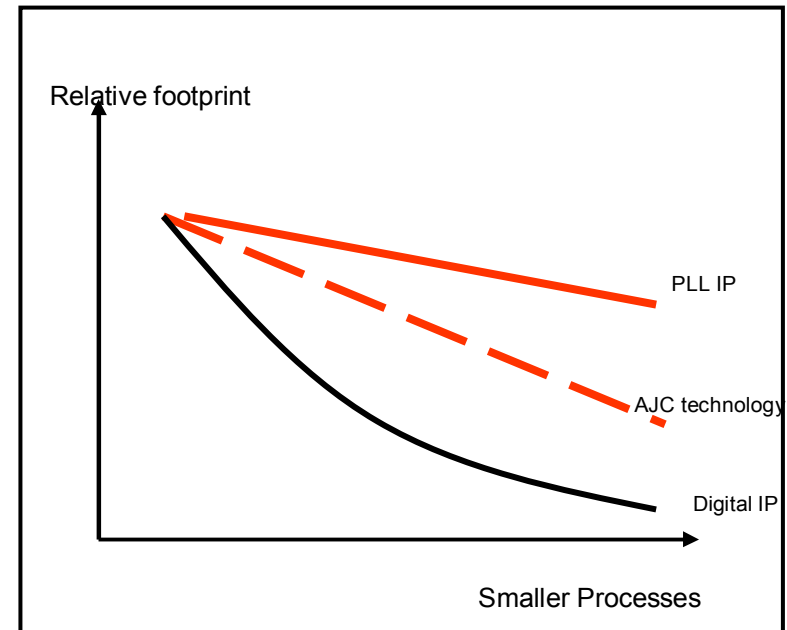
## Fine-grain (MCG)

- many voltage/frequency nodes
- continuous : no latency
- optimum cycles (bandwidth) usage
- software-friendly



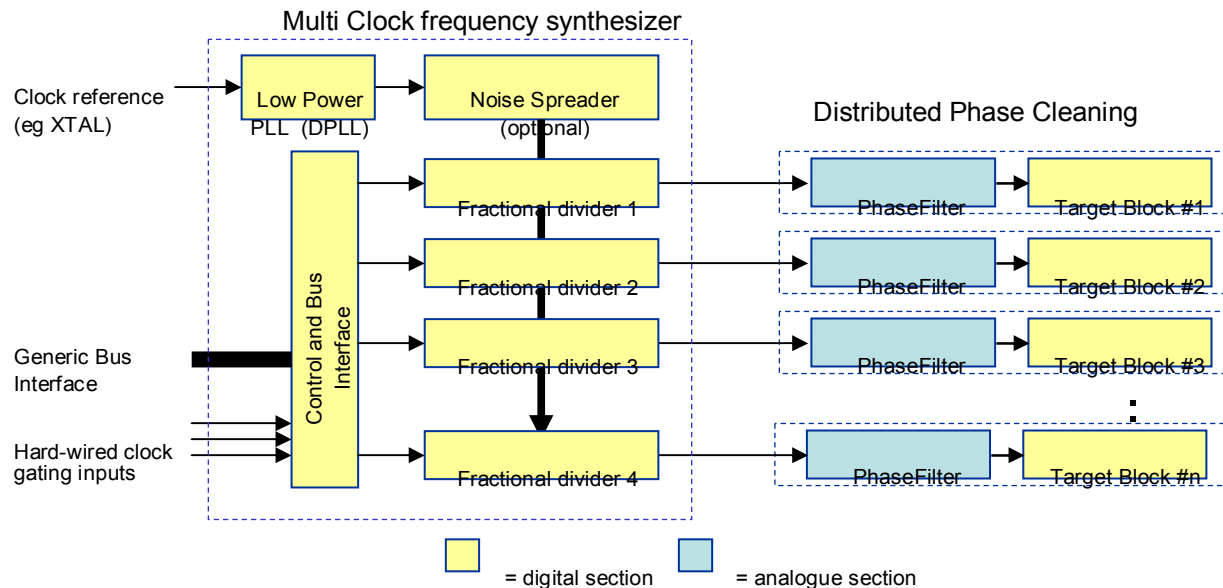
# Scalability of clocks

- PLLs
  - **don't scale down** with geometry
    - loop filter and inductors are nearly constant
  - **don't scale easily** across processes
    - need tuning to different processes
    - sensitive to physical environment
- SoC industry needs *scalability* in clock generation
  - creating & porting PLLs is a headache!
  - needs area-efficient solution




# Multi-Clock Generator (MCG)

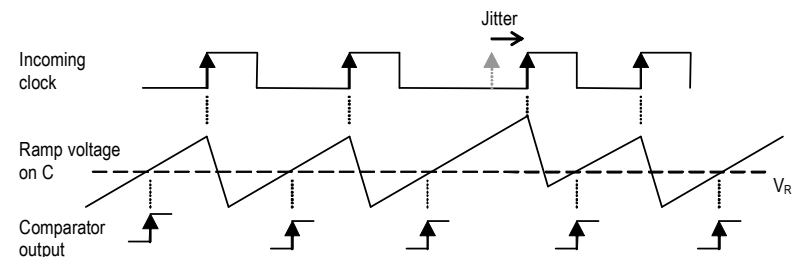
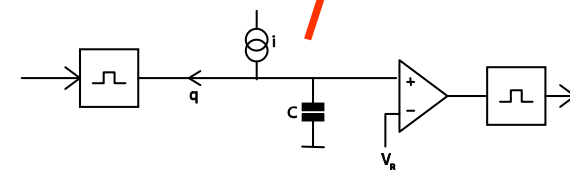
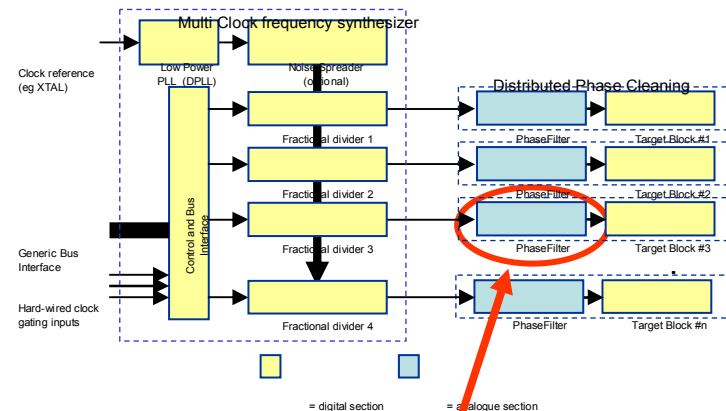
- designed for multi-core multi-clock domain SoCs
- low area, low power solution
- enables advanced DVFS power control
- single master PLL
- first silicon - Oct 2008



# AJC technology: creating a low-jitter clocks

**PhaseFilter** makes it all possible:

- converts jittered pulse train into a low jitter clock
- jitter bandwidth down to 10kHz
- operation up to 3GHz (90nm)
- -20dB to -30dB jitter suppression per stage
- AJC = anti-jitter cell: options for digital, DSP or RF quality
- lead customer: 

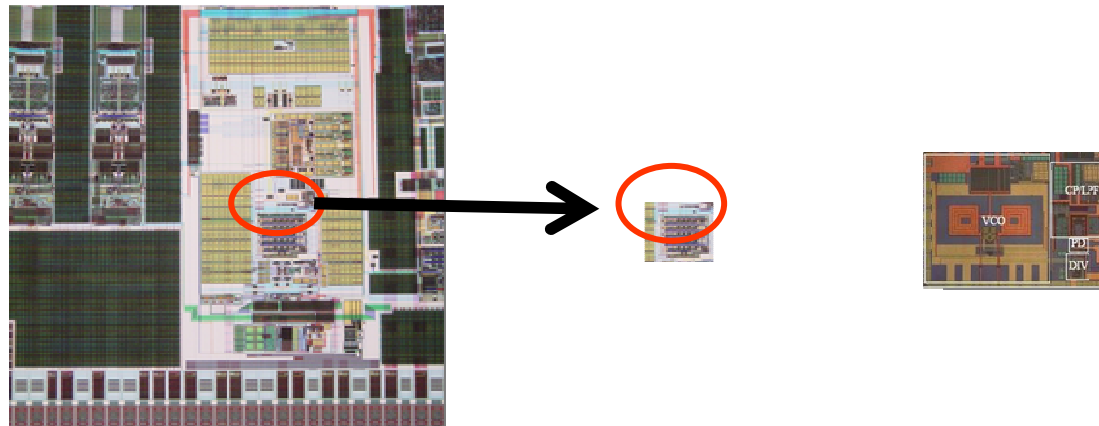


# AJC technology: compared to PLL

## AJC

- 1:1 frequency
- corrects *phase error* (jitter)
- a low-pass filter in the phase domain
- smaller footprint (no inductors)
- lower power (no VCO)
- frequency agile, instant lock

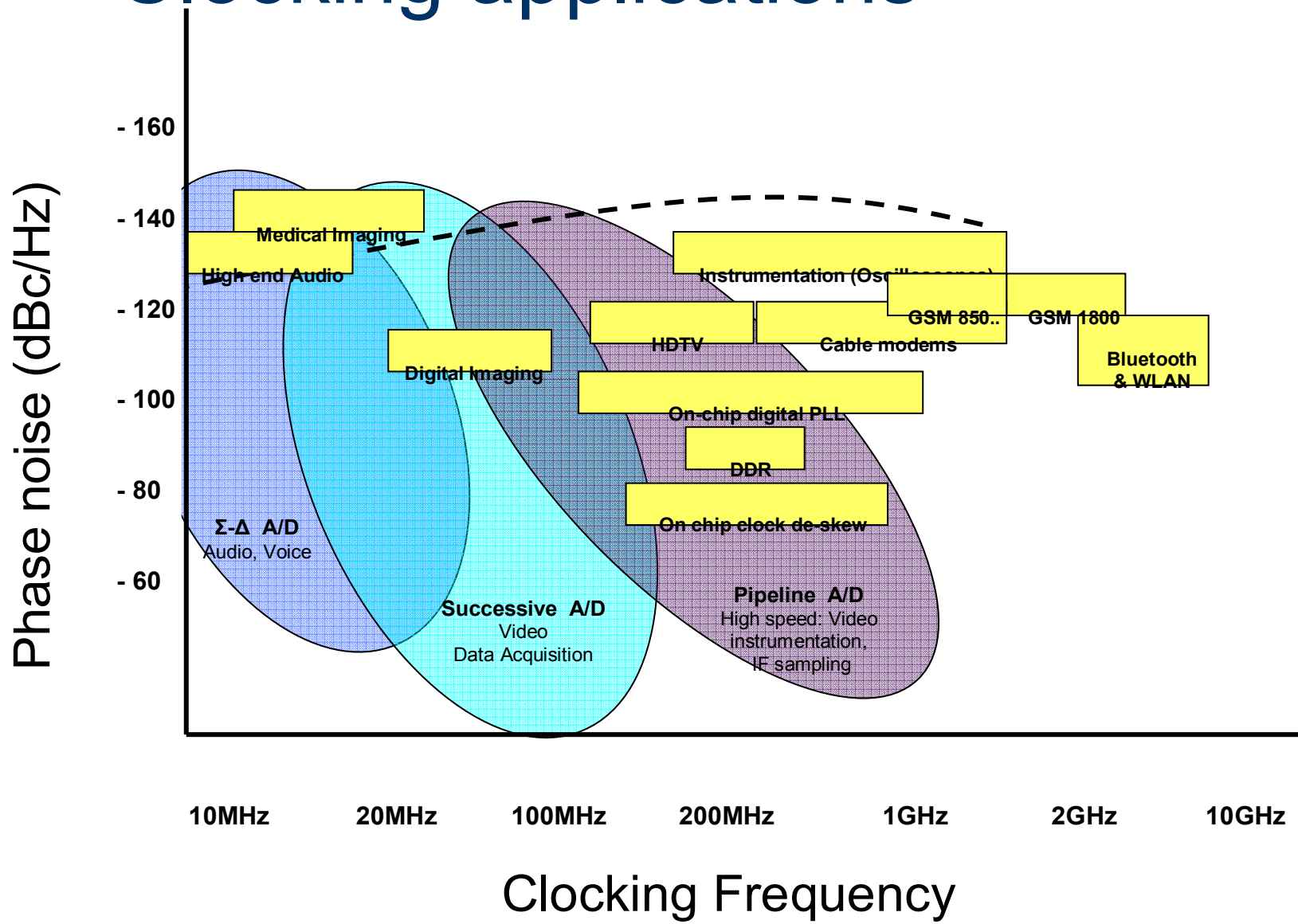
## footprint comparison (90nm)



four embedded AJCs

single PLL

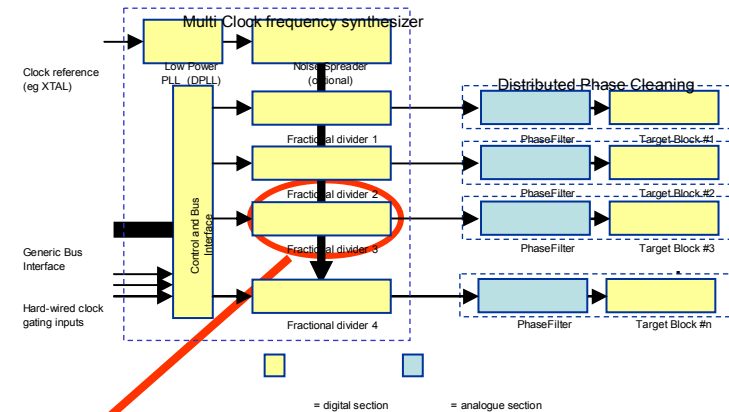
# Clocking applications



# MCG clock channel examples

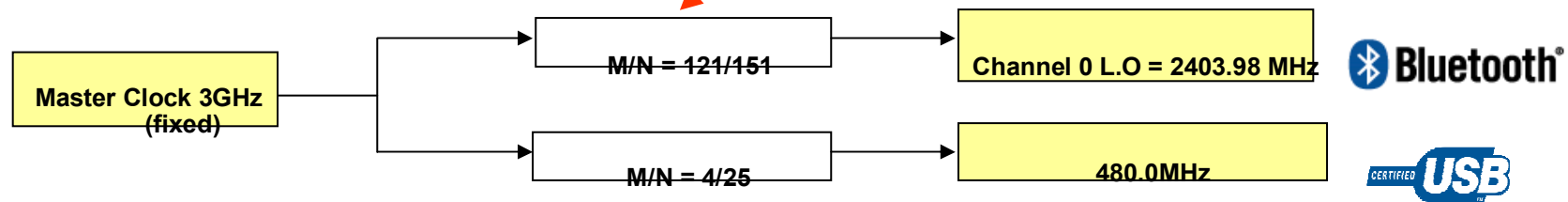
## Bluetooth LO synthesiser:

- 2.4 – 2.4835GHz, 1MHz channel spacing
- low IF: 2MHz
- frequency resolution required:
  - < 0.04%
- MCG resolution (M/N divider),
  - 64 bits: <0.01% with dithering



## USB 2.0 (Hi-speed)

- 480MHz clock
- frequency tolerance < 0.05%



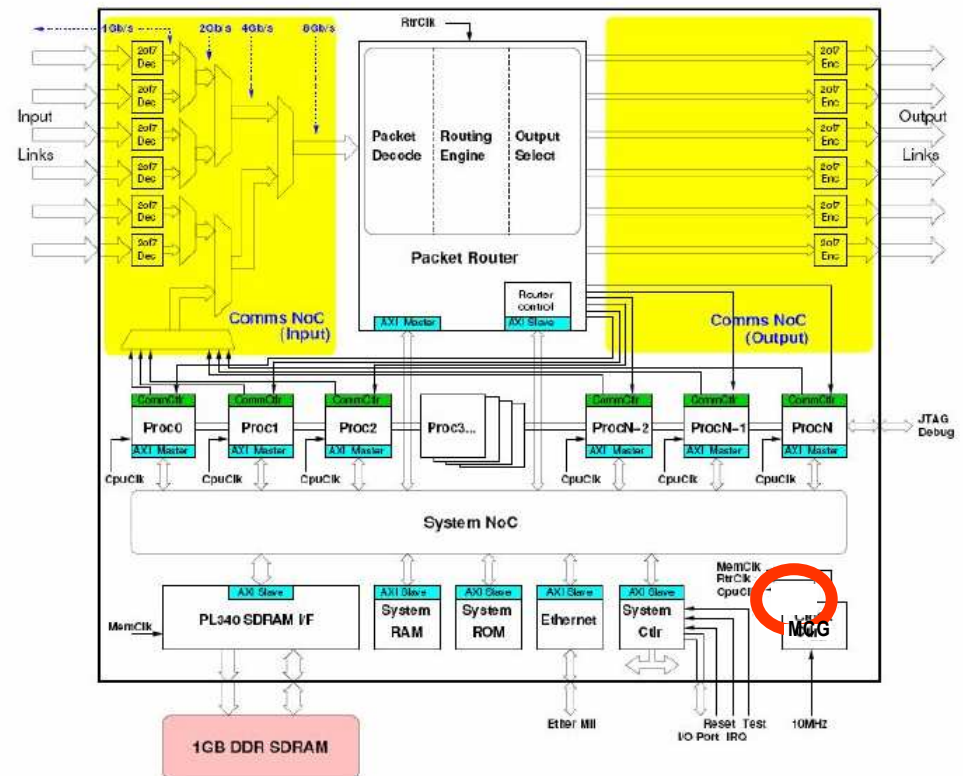
# MCG : design example

SpiNNaker: a multi-core NoC-based processor array for neuron simulation

- University of Manchester
- 20 x ARM968, I/O, router
- feature: asynchronous clock domains
- architecture scalable to future requirements: 200+ processors

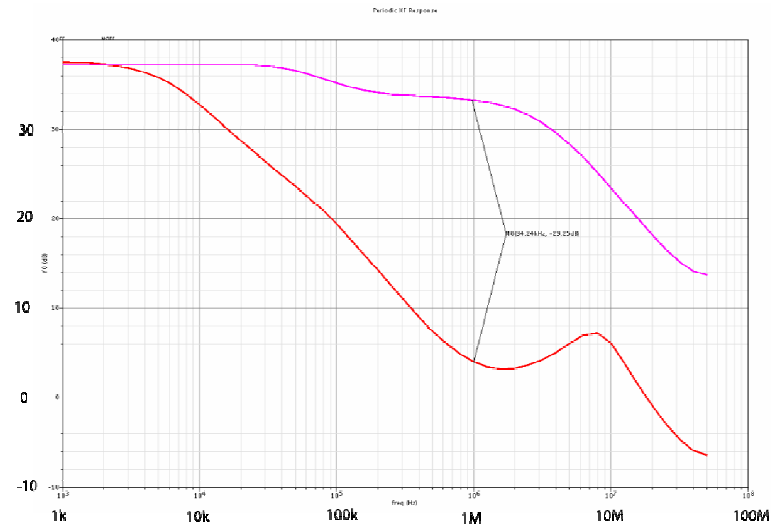
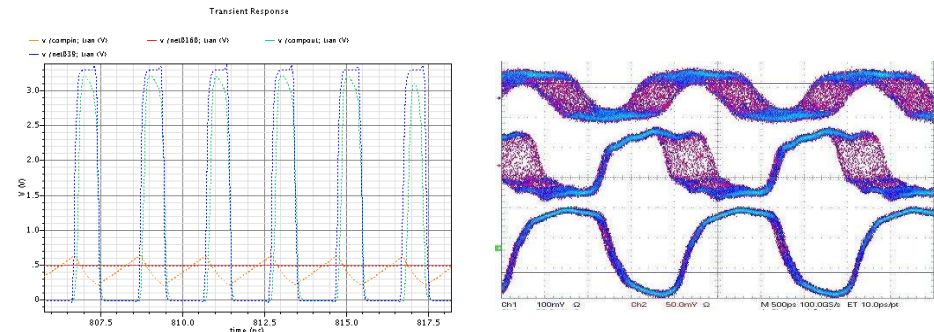
## SpiNNaker - clocking section

- multi-PLL based solution
    - 3.6 sq mm, 150mW
  - ... replaced by MCG
    - **1.2 sq mm, 35 mW**
- 66% less area, 76% lower power**



# AJC modelling: periodic steady state

- simple but challenging
- a linear circuit with complex voltage- and phase-domain characteristics
- long-term vs short term response modelling
- *PSS analysis* in Virtuoso
- Cadence EMEA team developed methodology for performance analysis
- simulation time reduced:  
15hrs → 30 mins



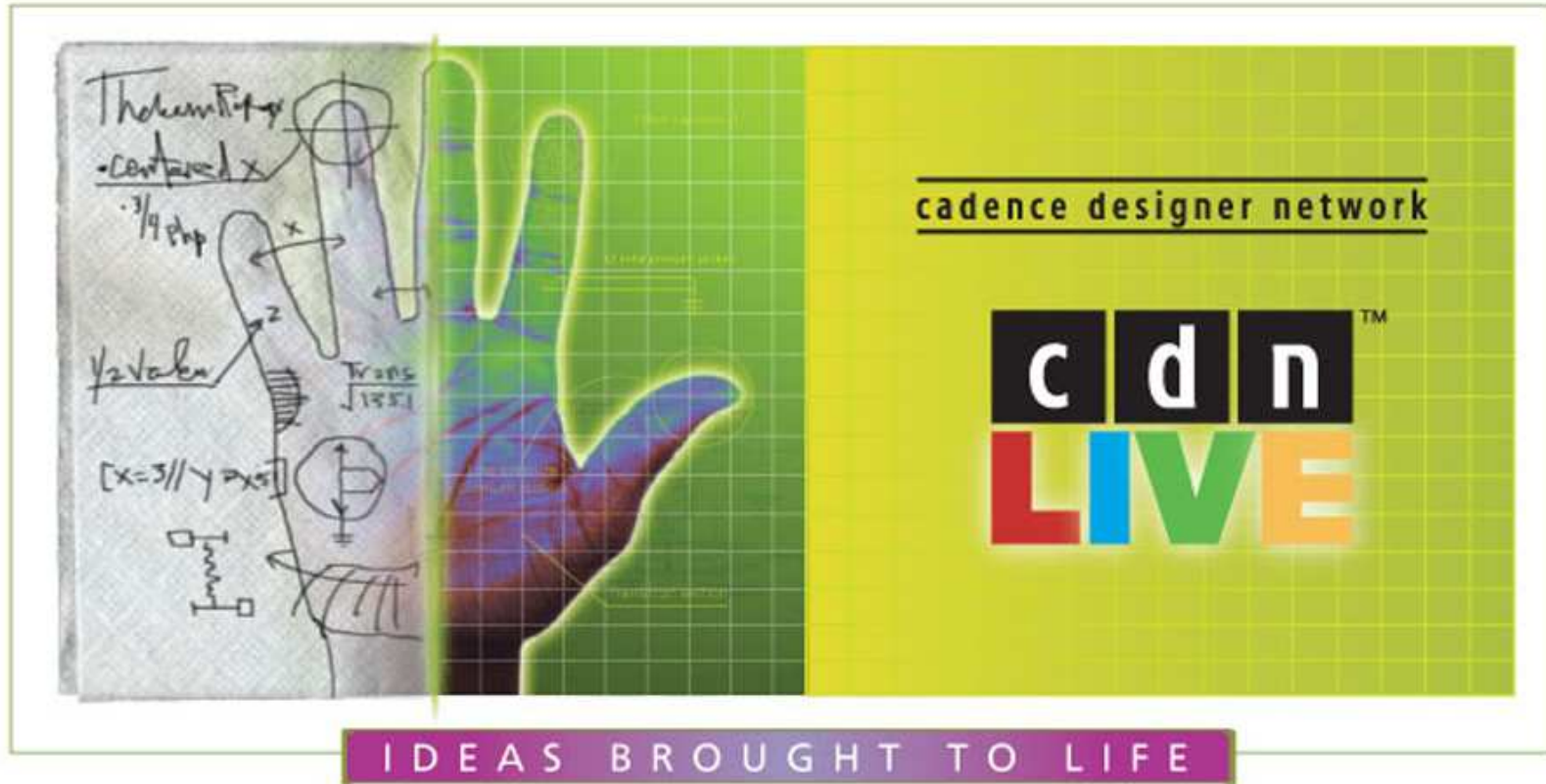
# Summary

- MCG is a versatile low-power multi-clock solution
- scaleable, modular, reusable, area/power efficient
- ideal where multiple PLLs ( $>2$ ) are needed

*Key simulation methods (AJC) developed in association  
with Cadence EMEA*

## Questions?

 cādence™



Theorem P1  
-contoured x  
3/4 step  
1/2 valve  
[x=3//y=2x5]  
Trans 1351

cadence designer network

cdn™  
LIVE

IDEAS BROUGHT TO LIFE



# About Toric

- founded 2002: from University of Surrey
- privately funded: IP development & licensing
- primary products:
  - AJC (Anti Jitter Cell)
  - MCG (Multi Clock Generator)
- innovative embedded clock technologies:
  - power saving, cost saving

