Hybrid Platform Application in Software Debug

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Software costs in SoC development

Software is fastest growing component of SoC development cost

Impact of Design Technology on SOC
Consumer Portable Implementation Cost

- Hardware Costs
- Software Costs

$ US Millions

2009 2010 2011f 2012f
Early software adoption

### Previous Development Process

- **IC Development**
  - RTL Design
  - Physical Design
  - Rev A0 Tape-out & Fab
  - Rev A0 IC Bring-up Validation, Debug
  - RTL Bug-fix & Feature Add
  - All-Layer Rev IC Validation
  - RTL Bug-fix
  - Metal Rev IC Validation
  - Qual Tests
  - IC Mass Production
  - Customer SOC Launch

- **SW Development**
  - Platform SW Development on SOC
  - Customer Validation & Network Integration
  - Ship SoC with poor Quality SW

### New Development Process

- **IC Development**
  - RTL Design
  - Physical Design
  - Rev A0 Tape-out & Fab
  - Rev A0 IC Bring-up Validation, Debug
  - RTL Bug-fix
  - Metal Rev IC Validation
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  - IC Mass Production

- **SW Development**
  - SW Development on Emulator/FPGA
  - Platform SW Integration on SOC
  - Customer Validation & Network Integration
  - Customer SOC Launch

SW Early Entry

High SW quality and cycle time reduction due to early SW adoption
Challenges for early software adoption

- SW teams have become the long pole in delivering SOC on time and with high quality
  - Exploring Fixed Virtual Platforms for early SW Development
  - Full Virtual Prototypes have a high cost of entry and lack accuracy

- Current Emulation solutions are too slow for the OS Based SW tasks

- Meeting SW teams needs with FPGA Prototypes becoming more difficult
  - Earlier access can only occur with "dirtier" RTL, which is difficult with FPGA compile times and challenging debug
  - Increased design complexity of multi-core/multi-cluster is exceeding the capacity of FPGA systems
Early, High-Performance SW Execution on Palladium

Exclusive solution combines the best characteristics of emulation and virtual platforms

TLM Virtual Platform – VSP
- Up to 100MHz
- Early availability for SW developers
- Advanced SW debug
- Fast SW turnaround time

RTL Emulation – Palladium® XPI/II
- Up to 4MHz
- From early-RTL to full-SoC validation
- Advanced HW debug
- Fast HW turnaround time

Cadence Hybrid Solution
- Boot complex OS at 48MHz
- Speed up SW-driven tests 1-10X over emulation
- Early availability for SW developers
- Advanced HW + SW debug
- Fast HW and SW turnaround time
Improved HW/SW debug capability

VSP Source Code Debugger

IES/Palladium HW Signal Debuggers

VSP HW/SW Memory Access

VSP Smart Message Logging

Interconnected
- Integrated processes
- Coordinated execution
- Unified Control
- Zero-time access to HW mem

Virtual Terminal

Linux Rehs Root
The Palladium/VSP Hybrid Solution

The Palladium/VSP Hybrid addresses the need for fast execution speed, to boot operating systems and execute applications. It does this by replacing the RTL CPU and memory with a virtual model that runs 50 times faster.

Architected for SW Performance
- High-speed virtual platform
- Asynchronous HW/SW Execution with Interrupt driven sync
- High-Speed Multi-Domain Memory Coherency

Designed to integrate HW and SW flows
- Does not require changes to HW or SW stacks
- Virtual connections into SW Engineer’s environments
- Seamless hybrid execution for both HW and SW users
Palladium Hybrid Focus:
Kernel, Drivers, Android, Linux-based tests
Hybrid Components and Insertion

- **Virtual Comps**
  - ARM Fast Model
  - Smart Memory (systemc part)
  - Re-configurable router model, etc.

- **RTL Comps**
  - Rest RTLS (removed cpu core and replaced memory by smart memory model)

- **Bridge Comps**
  - TLM/RTL Bridge
  - Reset and interrupts Manager

- **SWI packages makes it easier to do CPU and memory Hybrid integration**
Hybrid at SPREADTRUM

The following diagram shows all the components in Whale Hybrid environment:

Usage:
- Boot kernel
- Boot OS
- Run real world applications
- Run benchmark
Performance Result

- Linux kernel boot
  - Palladium only = 1 hour
  - Hybrid = 60 secs

- Android
  - Palladium only = Hours*
  - Hybrid = 6 mins
Conclusion

- Enables high-performance execution of SOC SW with RTL and is suitable for bare mental SW, OS, device drivers, test applications on OS.

- Enable co-develop and co-verify pre-silicon HW designs.

- Run Linux kernel boot and android boot near FPGA speed.

- Has advanced debug tools to facilitate SW debug and HW debug.

- High quality SW on silicon arrival and contribute to smoother bring-up

- Cut down time from design to market.
THANK YOU!